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VOLUME II
IMS Study Results Appendixes

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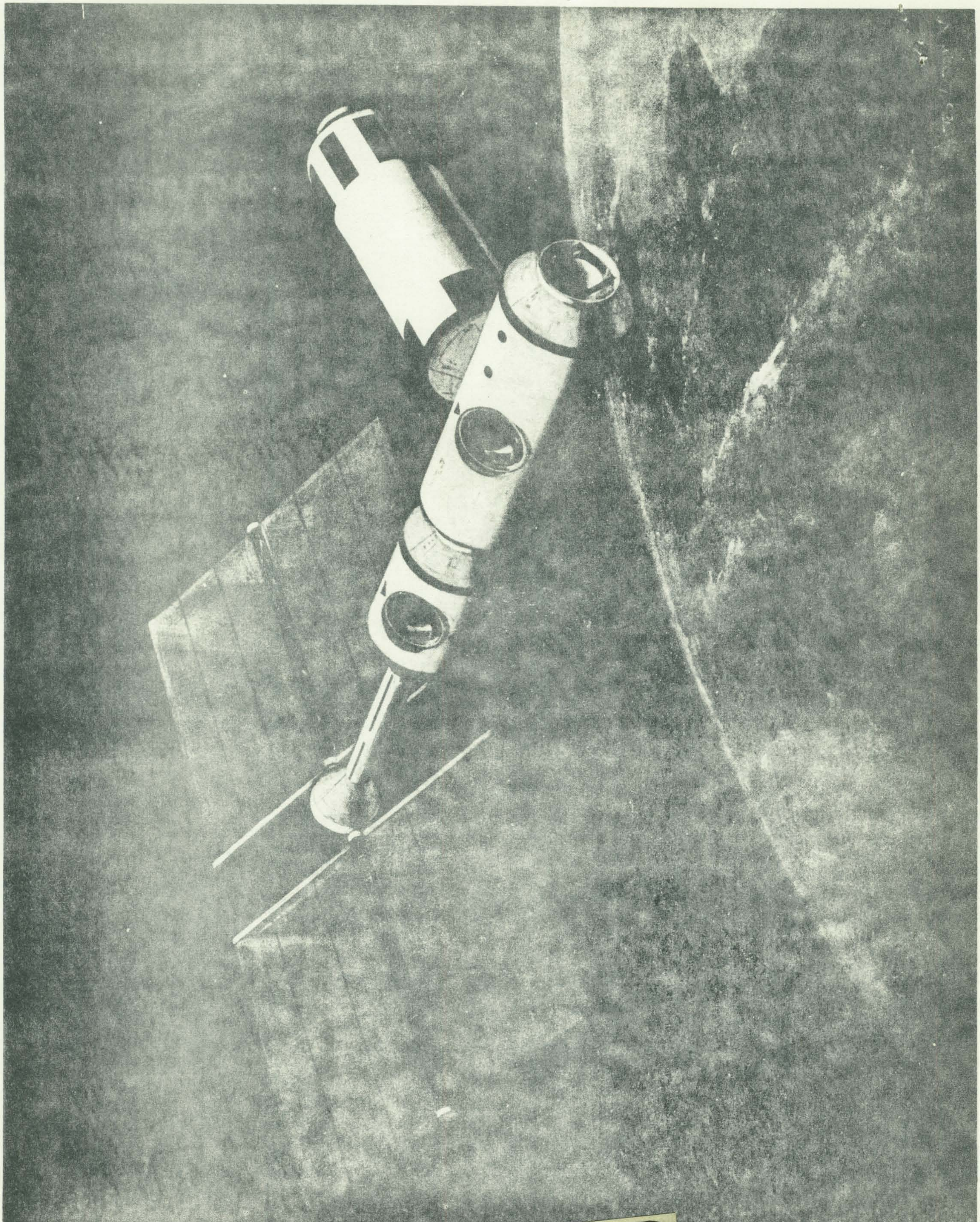

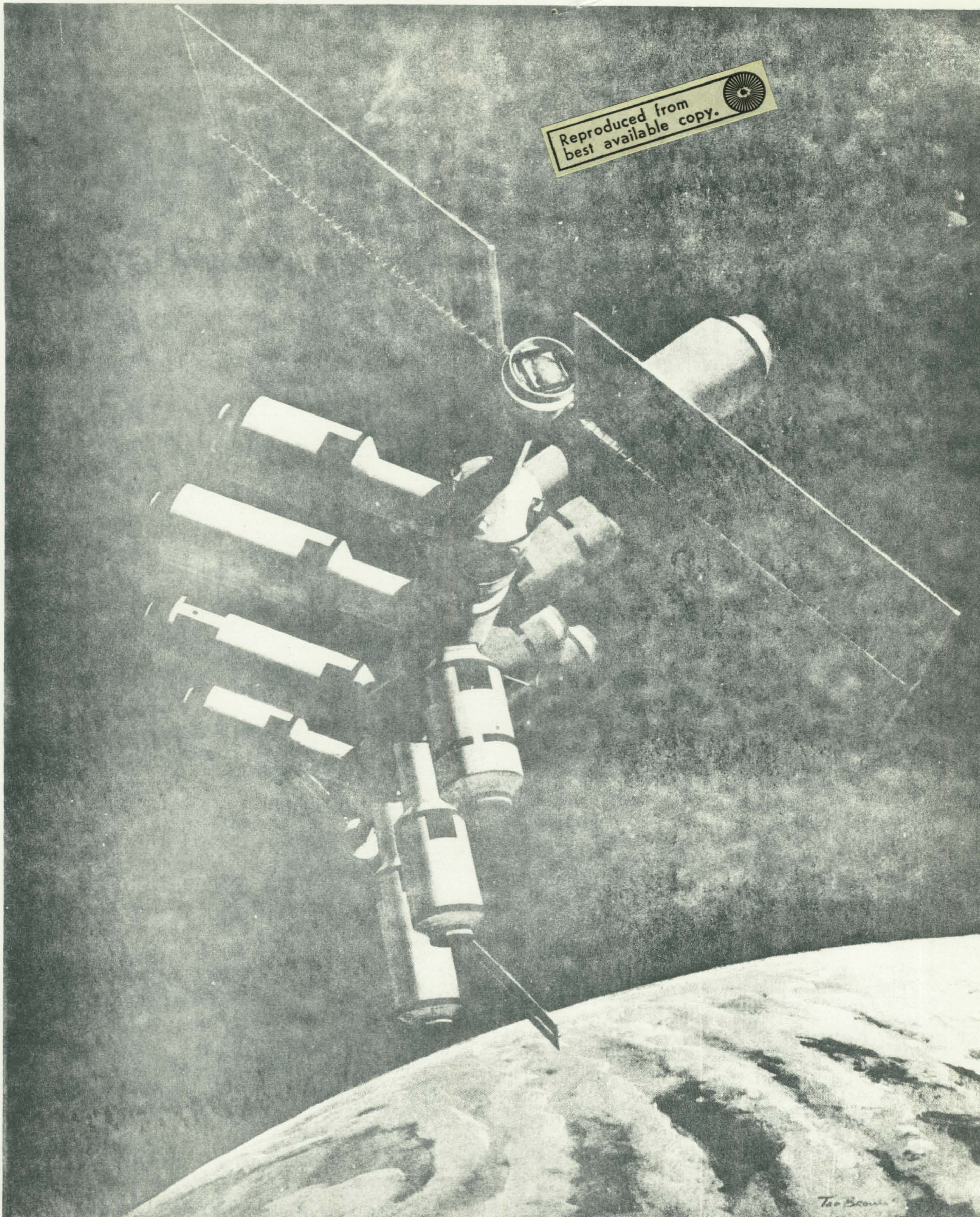
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PREFACE

The work described in this document was performed under the Space Station Phase B Extension Period Study (Contract NAS8-25140). The purpose of the extension period has been to develop the Phase B definition of the Modular Space Station. The modular approach selected during the option period (characterized by low initial cost and incremental manning) was evaluated, requirements were defined, and program definition and design were accomplished to the depth necessary for departure from Phase B.

The initial 2-1/2-month effort of the extension period was used for analyses of the requirements associated with Modular Space Station Program options. During this time, a baseline, incrementally manned program and attendant experiment program options were derived. In addition, the features of the program that significantly affect initial development and early operating costs were identified, and their impacts on the program were assessed. This assessment, together with a recommended program, was submitted for NASA review and approval on 15 April 1971.

The second phase of the study (15 April to 3 December 1971) consists of the program definition and preliminary design of the approved Modular Space Station configuration.

A subject reference matrix is included on page v to indicate the relationship of the study tasks to the documentation.

This report is submitted as the appendixes to Data Requirement SE-02.

DATA REQUIREMENTS (DR's)
MSFC-DPD-235/DR NOs.
(contract NAS8-25140)

Category	Designation	DR Number	Title
Configuration	CM	CM-01	Space Station Program (Modular) Specification
		CM-02	Space Station Project (Modular) Specification
		CM-03	Modular Space Station Project Part I CEI Specification
		CM-04	Interface and Support Requirements Document
Program Management	MA	MA-01	Space Stations Phase B Extension Study Plan
		MA-02	Performance Review Documentation
		MA-03	Letter Progress and Status Report
		MA-04	Executive Summary Report
		MA-05	Phase C/D Program Development Plan
		MA-06	Program Option Summary Report
Manning Financial	MF	MF-01	Space Station Program (Modular) Cost Estimates Document
		MF-)2	Financial Management Report
Mission Operations	MP	MP-01	Space Station Program (Modular) Mission Analysis Document
		MP-02	Space Station Program (Modular) Crew Operations Document
		MP-03	Integrated Mission Management Operations Document
System Engineering and Technical Description	SE	SE-01	Modular Space Station Concept
		SE-02	Information Management System Study Results Documentation
		SE-03	Technical Summary
		SE-04	Modular Space Station Detailed Preliminary Design
		SE-06	Crew/Cargo Module Definition Document
		SE-07	Modular Space Station Mass Properties Document
		SE-08	User's Handbook
		SE-10	Supporting Research and Technology Document
		SE-11	Alternate Bay Sizes

SUBJECT REFERENCE MATRIX

LEGEND:
- CM Configuration Management
- MA Program Management
- MF Manning and Financial
- MP Mission Operations
- SE System Engineering and Technical Description

	CM				MA		MF	MP			SE								
	CM-01 Space Station Program (Modular) Specification	CM-02 Space Station Project (Modular) Specification	CM-03 Modular Space Station Project Part I CEI Spec	CM-04 Interface and Support Requirement Document	MA-05 Phase C/D Program Development Plan	MA-06 Program Option Summary Report	MF-01 Space Station Program (Modular) Cost Estimates Document	MP-01 Space Station Program (Modular) Mission Analysis Document	MP-02 Space Station Program (Modular) Crew Operations Document	MP-03 Integrated Mission Management Operations Document	SE-01 Modular Space Station Concept	SE-02 Information Management System Study Results	SE-03 Technical Summary	SE-04 Modular SS Detailed Preliminary Design	SE-06 Crew/Cargo Module Definition Document	SE-07 Modular Space Station Mass Properties Document	SE-08 User's Handbook	SE-10 Supporting Research and Technology	SE-11 Alternate Bay Sizes
2.0 Contractor Tasks																			
2.1 Develop Study Plan and Review Past Effort (MA-01)																			
2.2 Space Station Program (Modular) Mission Analysis								●											
2.3 Modular Space Station Configuration and Subsystems Definition														●					
2.4 Technical and Cost Tradeoff Studies							●												
2.4.4 Modular Space Station Option Summary											●								
2.5 Modular Space Station Detailed Preliminary Design														●					
Mass Properties																●			
2.6 Crew Operational Analysis									●										
2.7 Crew Cargo Module															●				
Mass Properties																●			
2.8 Integrated Mission Management Operations										●									
2.9 Hardware Commonality Assessment													●						
2.10 Program Support					●														
2.11 Requirements Definition																			
Space Station Program (Modular)	●																		
Space Station Project (Modular)		●																	
Modular Space Station Project–Part 1 CEI			●																
Interface and Support Requirements				●															
2.12 Plans					●														
2.13 Costs and Schedules							●												
2.14 Special Emphasis Task Information Management (IMS)												●							
Modular Space Station Mass Properties																●			
User's Handbook																	●		
Supporting Research and Technology																		●	
Technical Summary													●						
MOD 29																			●
MOD 40						●													

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Appendix A

PRELIMINARY PART I CPCEI SPECIFICATION FOR THE SUMC EXECUTIVE PROGRAM

A.1 SCOPE

This specification establishes the requirements for performance, design, test, and qualification of computer programs identified as the SUMC executive program for the Modular Space Station (MSS).

The computer program contract end item (CPCEI No. TBD) consists of programs and supporting information required to support on-board application programs in one or more processing configurations (simplex or multiprocessor) operated as a single data management subsystem.

A.2 APPLICABLE DOCUMENTS

The following documents (tentative list) of exact issue shown, form a part of the specification. In the event of conflict between documents referenced here and detailed contents of Sections A.3, A.4, and A.10, the detailed requirements in Sections A.3, A.4, and A.10 shall be considered superseding requirements.

A. MSFC Advanced Aerospace Computer. Report No. SP-232-0384, 6 July 1970.

B. Data Processing Requirements SE-02, Section 2.1.1

C. Instruction Set Definition; SE-02, Section 2.3

D. Multiprocessor System Configuration; SE-02, Section 2.1.3

A.3 REQUIREMENTS

This section specifies the performance and design requirements for the SUMC executive program for the data management subsystem of the Modular Space Station. The subsystem is defined as being made up of one or more SUMC systems operated as simplex or multiprocessor systems, interconnected (distributed) with the Space Station data bus. Additional communications and controls exist in the multiprocessor systems to permit partitioning and operation as multiple simplex systems.

The following paragraphs refer to a set of units operating as a multiprocessor, simplex, or simplex partitioned multiprocessor.
The executive program design shall accommodate the three basic processor configurations with automatic programmed switch at least between the multiprocessor and partitioned configurations. The distributed systems may reside in any Space Station module or any attached experiment or free-flying module. The program organization shall be such that ground support systems can tailor the executive program to meet requirements of individual processors.

A.3.1 Performance

The executive shall control and monitor the utilization of DMS resources by Space Station application programs and ensure the high availability and usability of the DMS processing capability. The permitted degradation will be consistent with the stated design objectives relating to reliability, flexibility, and modularity. Common functions or services will be provided by the executive when it can be clearly demonstrated that the centralized approach will result in cost reduction, improved performance, or increased likelihood of total mission success. Total system optimization will be stressed by the establishment of the following major objectives.

A. Control and Monitor—The executive program shall control all DMS resources and maintain the status of all programs in a multiprogramming environment, and in a multiprocessing environment if required by the processor configuration. Scheduling algorithms will be included that consider program priorities, timing requirements, availability of input, and DMS status and current DMS utilization factors. Utilization measurements or statistics and checkpoint or log recordings will be accumulated consistently with the current activity level and external requests. The most recent measurements will be available for display to the crew or for automatic controls in the executive or application programs.

B. Reliability—The functions provided by the executive shall be structured in such a way that detected and undetected errors in secondary functions and application programs will have minimum impact on primary or more-critical processing functions. The error sources included are hardware or software as well as those originating in system specifications. The approach shall permit the level of testing and verification of components to be consistent with the availability requirement of the component or associated function.

C. Flexibility—The executive shall include functions to permit concurrent development of many application programs without explicit knowledge of unit or channel addresses and processing techniques of other applications. The addition, deletion, or modification of DMS units should have minimum impact on application programs.

Executive processing functions such as program scheduling shall be alterable to accommodate different mixtures of periodic and event scheduled application processing, either of which may have real-time constraints. General capabilities to conserve main storage may include, but not be limited to:

1. Program module sharing among applications.
2. Application program segmentation and dynamic loading.
3. Auxiliary memory communication or data queues.
4. Resource availability tests for applications.

D. Modularity—The executive program will be structured such that components relating to particular configurations, functions, or components can easily be modified, redefined, or omitted without redesigning other components. The design shall permit the automatic generation of the executive program for various simplex and multiprocessor configurations by ground support programs and the reconfiguration from multiprocessor to a single or multiple simplex operation in flight. The latter will occur as a result of manual or external request, or will be automatic upon detection of a failed component.

The executive shall continue to operate and control a predefined subset of system functions with processor degradation to a single CPU, a single IOC, and a single main memory unit. A nondestruct or auxiliary memory unit is not required if the processor is normally restarted with a program load over the data bus, controlled by another CPU or telemetry and power interface.

E. Common Functions or Services—The capability shall be included to permit functions of the executive or application programs to be implemented as a set of subprograms to minimize the main memory requirement for peak processing periods and to take advantage of available memory during off-peak periods. Re-entrant or serially reusable (closed) routine pools will be supported by the executive to decrease memory requirement. The functions may include but not be limited to:

1. Mathematical or general digital processing.
2. Auxiliary or bulk memory support.
3. Subprogram loading by application request.
4. Intra- or intersystem/program communication control.
5. Program development or test support.
6. Dynamic data checkpointing and recovery/restart.

A.3.1.1 System Requirements

The executive program design shall facilitate the development, testing, and on-board execution of Space Station subsystems and experiment application programs. Each processor shall be initially loaded by an interface with an operating processor or other external signal. In the case of a multi-processor, the initial load may result in a simplex configuration, which will be expanded under programmed control to a multiprocessor or simplex partitioned processors. Initializing a simplex partitioned processor shall always be under programmed control if the multiprocessor is accomplishing an operational function.

The executive program will be structured as a heirarchy of subprograms defined to meet the objectives listed in Section A.3.1, of which the highest or highest subset has primary control over primary or critical DMS functions. The control hierarchy is to insure that most complex processing functions and the majority of all program logic can be isolated from primary system control function in the event of detected and undetected failures. Either may imply nonisolated error conditions.

Application programs are supported through an interface similar to secondary subprograms of the executive. In addition to isolation, the structure will permit more efficient response to application program demands of high priority with respect to certain secondary executive functions. Application program hierarchy will be utilized to simplify isolating program responsibility during anomalous processing, status recording, or while preparing status displays for the crew.

A.3.1.1.1 System Management

The executive program will configure or reconfigure a processing subsystem from a set of intraconnected units made up of the following unit types and channels up to the maximum numbers specified:

A. Central processing unit (4).
B. Input/output control unit(3).
C. Main memory units (15).
D. Auxiliary memory units (4).
E. Data bus channels (8).
F. Auxiliary memory channels (2).
G. Alternate auxiliary memory channels (2).

The program structure and control organization will be such that the majority of reconfigurations from single unit failures can be accomplished in less than TBD milliseconds exclusive of checkpoint data retrieval. System management shall include any of the following types of services:

A. Processor reconfiguration.
B. Initial program loading.
C. Interrupt processing.
D. Centralized status or error monitoring.
E. Register conditioning and control of DMS units.
F. System log (data or statistics recording).
G. System debugging aids (hardware or software).
H. Control of common subprograms or data.
I. Intra- or interprocessor communication control.

Control constants or variables resident in main memory and relating to one processor will be referred to as the "system control table." The table may have continguous locations or in a list structure but sets of information relating to particular functions will be referred to as "system (function name) control blocks."

A.3.1.1.2 Program Management

Program control shall be provided for program load, initiate, scheduling, execution, and termination processing of all executive subprograms and application programs. Up to TBD unique program definitions will be permitted, each of which may involve up to TBD subprograms in an established hierarchy. Subprograms may contain SUMC instructions, tables, or dynamic variable sets and will be referred to as modules in subsequent paragraphs.

Each module will contain a program control block containing descriptive information and control constants or variables. Once loaded, the program control block will be modified only by executive control logic. The program control blocks will be utilized to construct task control blocks for all top-level program modules having direct responsibility of resources assigned by the executive. The task control block will contain control constants or variables associated with the corresponding program and will be resident in main memory between the time of initiation and termination.

Common control constants or variables relating to modules or tasks will be retained in a task control table or a program control table. The tables may be defined as contiguous memory locations or as a scattered (list) structure, but in both cases, the logical elements corresponding to individual modules or tasks will be referred to as task control blocks or program control blocks.

A.3.1.1.3 Resource Management

The total processing capability of the data management subsystem (DMS) can be thought of as maximum utilization of all DMS units allocated in an optimum fashion to a set of application programs. DMS resources include memory space and control processing unit or channel time. General resource allocation or control functions may be defined to accommodate similar requirements in application processing relating to any Space Station subsystem.

A.3.1.1.4 Input/Output Management

The set of program functions shall provide services associated with access or communication control of all input/output controller units, data bus channels, data bus terminals or attached units, and auxiliary or bulk memories. The program shall accept requests for single or multiple communication sequences to be accomplished on demand or at specific time intervals. Time intervals may be as short as 10 milliseconds or multiples of some TBD common base time interval.

A.3.1.2 Operational Requirements

The Space station digital data processing includes guidance, navigation, attitude control, DMS maintenance, on-board subsystem checkout, and other more detailed requirements described in documents previously listed (Section A.2). The on-board programs implemented to meet total Space Station processing requirements are identified as application programs that operate under control of an executive program that has prime responsibility for the integrity and effectiveness of the DMS.

To meet the system requirements, the executive program will be defined such that minimum logic is required to exercise primary control over the data management subsystem. Figure A-1 depicts the primary control flow among the major processing functions. The control flow and secondary executive functions will be arranged in such a way that hardware-assisted isolation of executive functions can be implemented as well as isolation of specific application functions. The requirements for the executive will be discussed by major function in the following paragraphs.

A.3.1.2.1 System Management

The subfunctions may include any routine or shared processing sequence whose common definition tends to reduce system complexity and increase system flexibility, visibility, and reliability as well as providing the

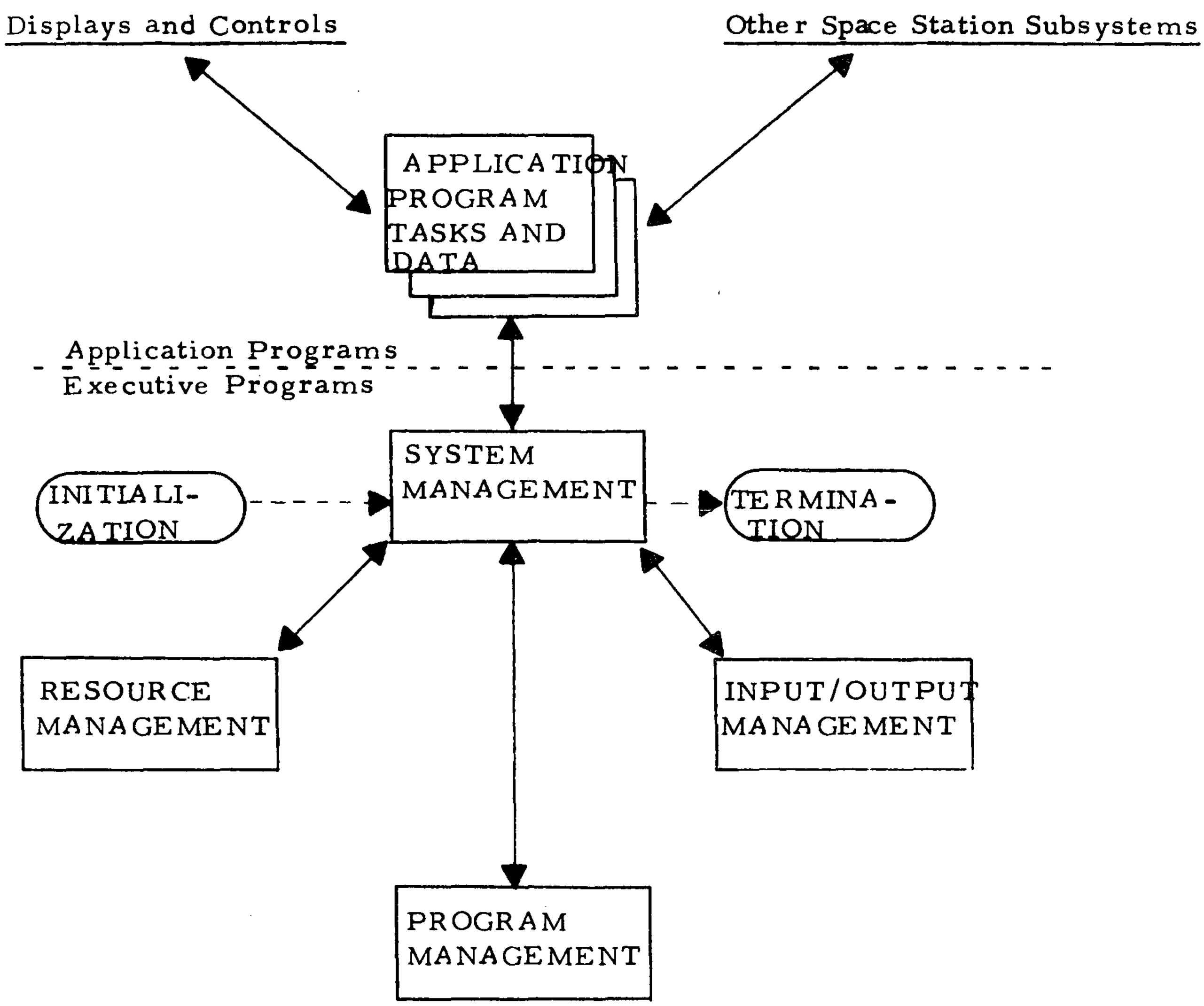


Figure A-1. Primary Control Flow

required top-level DMS sequencing operations. The subfunctions will at least provide the following types of capabilities:

A. System Initiation/Reconfiguration/Termination—Provides for the initialization of a particular SUMC processor of DMS and system-level alterations during a period of operation, and accomplishes a shut-down sequence at termination of a period of operation.

B. Interrupt Processing —To save machine status, analyze status information, post completion of anticipated interrupt or micro-programmed internal traps, record all unanticipated interrupts, and restore machine status or pass control to a CPU dispatching routine.

C. Dispatching—An available CPU to the next processing function to be accomplished based on current system status and scheduling parameters preestablished by program management.

D. Common Services—Are provided for application programs and executive subprograms or routines such as system control table updating, event or timing signals, message handling for inter- or intraprocessor system communication, power conservation sequences, or any frequently used processing function that may be coded as a re-entrant or reusable routine.

E. Status Monitoring—Statistics gathering, system log control and manipulations, and debugging aids to detect undesirable aspects of system operation and in general permit real-time analysis of on-board processing performance.

F. Centralized Control—Of processing sequences and error detection/recovery logic including incident recording in the system log and checkpointing. Checkpoint reloads of the executive and critical tasks are accomplished as required, and the requesting execution of system maintenance programs.

A.3.1.2.1.1 Input to System Management

Input in the form of requests for services including messages to be forwarded to the system log or other program tasks in the same or any distributed processor. An external signal will be accepted as a signal to accomplish system initialization, reconfiguration, or termination. Other sources of information are

A. Auxiliary memory.
B. System control table.
C. Program control table (and blocks as required).
D. Task control table (and blocks as required).

A.3.1.2.1.2 Output from System Management

Outputs consist of information placed in output parameters or variables associated with the request and possible updates to auxiliary memory or the system log. In addition, any table or control block listed above as input can be updated.

A.3.1.2.1.3 Processing

Details of the processing accomplished vary with the particular service provided. But except for the servicing of the external control signal and system control table updating, the request processing and information gathering functions are controlled by status information in the system control table. Requests to update key system parameters must come from the communications or displays and controls program or at least be verified through either of those programs. External signals or configuration control signals will be verified independent of application programs or by manual intervention, at least in the manned mode of operation. Key subfunction processing is described as follows:

A. System Initiation—Shall be accomplished by a microprogrammed sequence activated by a signal originating external to the processor. The signal will force one processor to preload configuration control registers to connect a CPU, an IOC, and at least one main memory unit. An I/O read request is then initiated to load a larger processor initiation routine from auxiliary memory or from a predefined terminal address. If the I/O completes normally, control is passed to the routine loaded. Otherwise, the sequence is repeated, alternating predefined addresses or configuration control variables TBD times before a configuration control reset is attempted. Initiation is not complete until basic executive, communications, and displays and control programs are activated. If a checkpoint restart is to occur, it is verified from information on auxiliary memory and accomplished during system initiation.

B. System Reconfiguration—May occur at any time following a successful system initialization. The request may come from DMS maintenance programs, the crew or from an internal executive function recognizing an interrupt indicating a specific CPU, IOC, or memory unit failure. The current operating status of the processor is maintained in a system configuration control block which contains the current status and parameters associated with each unit.

Parameters associated with reconfiguration requests are formatted in similar blocks which are used to replace the original blocks in the system control table. If the request is to partition a multiprocessor, the basic executive routines and queues are copied to the designated memory module before each configuration control register is modified. The reverse process is accomplished by assigning the designated partitioned processor's units to the currently controlling processor.

C. System Termination—Will be accomplished when a request is received from the crew or external command from a designated terminal source or remote processor. The termination routine will permit immediate termination of application programs leaving the executive program in a postsystem initiation state or immediate termination of all programs and power down of each unit. If auxiliary memory is available on the processor, the normal termination is to signal the request to predesignated application programs, delay a specified time period, checkpoint the executive queues, and proceed as with the immediate termination request.

D. Interrupt Processing—Is accomplished in the initial load routine to complete system initialization but during normal operation, interrupt processing routines will store system status relating to the interrupt. If the interrupt is expected, the appropriate system interrupt control block is examined to determine the action to be taken.

For power failure or other critical system indications, signals may be directed to other processors and error detection/recovery logic is executed immediately. Other interrupts may be flagged as acknowledged in the interrupt control block or designated queue entry and further processing delayed. In the latter case, processing will be resumed by the responsible task when selected by the CPU dispatch routine.

E. Dispatching—Will normally be entered directly from short interrupt processing routines to insure that most processing will be accomplished based on software assigned priorities without arbitrary distinction between executive and application functions. The dispatching function will modify system status by providing scratchpad memory content control, presetting hardware logic for data or instruction protection mechanisms, and assigning a CPU to the highest priority task ready for execution. The dispatching mechanism will permit selection of task from a queue dedicated to a particular CPU or a queue shared by more than one CPU.

F. Common Services—Such as control of a system log, program messages, or shared modules and are always controlled by system control table variables. Processing sequences are preestablished for dispatching by a system wait and post routine. The two routines manipulate control blocks that describe sequences that are waiting for some event and a queue of sequences that are ready for processing by a CPU. System log control and manipulation include switching on and off combinations of flags in the system control table and forcing the main memory log buffer areas to be recorded on auxiliary memory or be reused without recording. At least a double-buffer technique will be used to increase the log retention capability. When practical, unallocated main memory areas may be utilized to accommodate recording peaks. Requests to retrieve portions of the log or log control variables will be accomplished by display and controls programs.

Message queueing for program communication may utilize main or auxiliary memory and the queue will be serviced by a program communication routine of the executive operating as a task similar to an application program. The program control table is accessed to determine the routing required for a particular message. Intraprocessor messages are output on request from the receiving program, but interprocessor may be sent unsolicited or on request from the designated processor.

A.3.1.2.2 Program Management

The program management function will establish the current processing schedule and load, initiate, or terminate all program tasks. The task may be any processing function of the executive application, including:

A. DMS maintenance.
B. Experiment processing.
C. On-board checkout.
D. Flight operations.
E. Flight support.

The algorithms utilized in program management will insure adherence to resource limitation parameters contained in the system control tables. The tables are maintained by resource or system management, and the parameters include limits on space and processing time. The scheuling flexibility shall provide for immediate or queued requests for program management services.

Request to load a single or multiple program modules that contain program text (instructions, constants, variables, or any combination) will be serviced. If initiation is also requested, the program control block associated with the module is used to create a task control block. If initiation is not involved, the program control block and module responsibility are assigned to the requesting task. Termination processing involves insuring that resources assigned to the task are released or otherwise accounted for.

A.3.1.2.2.1 Input to Program Management

Input in the form of requests for services may originate from any program executing under control of the executive or from other functions or subprograms of the executive. All requests are associated with a task control block and except for queued initiations, the contents of the task control block and the corresponding program control block are accessible. Depending on the requested function, an event control block and the following information sources are also utilized:

A. Activity schedule table.

B. System control table.

C. Task control table.

D. Resource control table.

A.3.1.2.2.2 Output of Program Management

Outputs consist of information placed in output parameters or variables associated with the request and possible updates to:

A. Task control table.

B. Program control table.

C. Task control block (referenced and/or requesting programs).

D. Program control block (referenced and/or requesting programs).

E. Event control block (referenced or requesting programs).

F. System control table.

G. System log.

A.3.1.2.2.3 Processing

The program control tables will be maintained to indicate which programs (one program for simplex operation) are executing, ready to execute, waiting on an event or set of events, or in an inactive state. The latter also requires that information be maintained as to the memory and memory locations containing the program or program modules. Also, the conditions under which the program is to be automatically initiated by the executive or is allowed to be initiated by requests from other programs is maintained.

Requests for services, actions taken, and statistics relating to performance are recorded in the systems log as currently requested by flags in the system control table.

A. Task Scheduling—Or short term real-time program scheduling is accomplished from information contained in the system control table and temporary or permanent queues. Periodically, the activity schedule table is utilized to update the short- or near-term scheduling parameters. The activity schedule table is a top-level schedule for controlling the on-board experiment, subsystem, or manual activities. DMS maintenance is a support program function normally scheduled by crew request and is handled by the DMS executive program similar to any application program. The difference is that an interface will be defined to permit DMS maintenance to execute priviledged instructions and request configuration changes.

B. Task Initiation—Will normally occur as the result of servicing a system queue relating to a processor state change, elapsed time, a specific time, or other defined event. The state change may be a processor utilization level maintained by system management state flag modified by the crew through the display and control interface or changes in remote status monitored by I/O management. The program control table is referenced to establish the status of the program module referenced. If the module is in main memory and is inactive or is re-entrant, a task control block is initialized and is placed in a processor work queue. If the module must be loaded, control is passed to a memory content control routine.

C. Content Control—Processes requests to delete, load, or overlay program modules. Loading and deleting requires passing control to resource management to release or acquire main memory locations. If program overlay is involved, the location will be verified to be currently assigned to the requesting tasks.

D. Control and Support Subfunctions—Will be designed to permit application or executive tasks to:

   1. Execute—Standard routines controlled by the executive and made available to any application program to reduce main storage requirement.
   2. Load—A single or multiple program modules that contains instructions, constants, variables, or combination in a main memory location currently controlled by or dynamically assigned to the requesting task.
   3. Delete—Any program module or modules acquired by a load request and optionally return main memory responsibility to the executive.

4. Initiate—A program task and assign the responsibility to the requesting task or the executive. The program control table is referenced to validate the request and to locate the referenced program before accomplishing the task initialization function.
5. Terminate—A program task making the request or any referenced task whose responsibility is currently assigned to the requesting task.
6. Wait—Or delay execution or the requesting task until a specific time, elapsed time, event, or events have occurred. The request will be processed by the wait routine or system management and is associated with a system event control block. The control blocks will be chained to describe single or multiple conditions for subsequent execution of the task. The task is placed in the ready status when the executive has posted the last event required to satisfy the chained conditions.
7. Post—Will be accomplished by the corresponding system management routine when the requesting task references a system event control block in memory to which the task has data store privileges. The associated task will be removed from the waiting status if all of the chained conditions are satisfied or when the first unconditional event has completed.

E. Task Termination—Is accomplished by an executive task when a terminate request is received from another executive function or from an application program having responsibility for the referenced task. Checks are made to insure that system resources have been returned with exception of dictionary controlled memory locations. When the request is for self-termination, the main memory associated with the request reference is returned as a normal operation; all other purge operations are considered abnormal and will be handled by nonresident executive logic.

A.3.1.2.3 Resource Management

DMS resources include input/output channels and directly addressable main, auxiliary, or bulk memory locations. Any DMS unit or group of units that accomplish a specific function may be considered a resource. The set of resources will be monitored, controlled, or reassigned by the executive program manipulating resource description tables or data list structures describing the particular resource. Requests for resources shall be for immediate allocation or to be queued for resource availability based on a priority relationship among the requesting programs. By chaining system event control blocks, control may be returned to the task prior to allocation.

The resource management function will provide allocation control for any shared DMS resource by updating a resource control table, a specific resource control block, or system queue and thus provide a capability for application programs to coordinate usage of any shared Space Station resource and communication signal. In coordination with wait and post functions of program management, a general capability will be provided for the control of shared resources such as data tables, hardware units, and re-entrant or reusable program routines. At least the following major subfunctions will be included:

A. Immediate Allocation or Release—Of a standard size block or multiple blocks of main or auxiliary memory. Control of bulk memory usage shall be by use of generalized support functions.
B. Define or Delete a Temporary Queue—By name and insert, read, or remove an entry of a temporary or permanent queue.
C. Permit a Program to Test—The status of a particular queue or resource by returning information contained in the associated control block and to optionally enter a queue to seize and lock a control block on a shared or exclusive use basis.
D. Immediate or Queued Requests—For a real-time clock signal, an elapsed time signal, or other event that is associated with a common application or executive monitored event.
E. Resource Recovery—By relocation of allocated areas or by forcing release of a particular resource.

The queue mechanism shall permit main or auxiliary memory storage and at least the following entry ordering and servicing:

A. First in is first out.
B. Last in is first out.

C. Out by relative position.

D. Out by priority order.

A.3.1.2.3.1 Input to Resource Management

Input in the form of requests for shared or exclusive use of a resource or set of resources may originate from any program executing under control of the executive or from other functions or subprograms of the executive. The following information sources are also utilized and associated control blocks and/or queue entries:

A. Task control table.

B. Program control table.

C. System control table.

D. Resource control tables.

A.3.1.2.3.2 Output of Resource Management

Outputs consist of information placed in output parameters, resource control table, and the program control block associated with the requesting program. Any table or block listed as input may be updated.

A.3.1.2.3.3 Processing

Queues that are dynamically created and deleted are considered temporary and need not have the exact structure of a queue that is defined to accomplish a continuous function. The latter may be designed to permit a limited number of queued requests or no queueing and be organized to minimize overhead for such functions as main memory or processor allocation.

Each queue defined is associated with an executive control program routine that services the request or that performs general queue maintenance functions. Routines such as memory allocation shall be designed to minimize fragmentation of memory space and retain an allocation table such that statistics on memory usage can easily be extracted. Memory space shall be recovered quickly even though a failure occurs in a particular program with space currently allocated.

The attributes of the queues and chained queue entries are dependent on the requrements of the function to be accomplished and the queue service routine.

Examples of attributes are:

A. Queue identification.

B. References to responsible program or particular service routine.

C. Priority or precedence and request related parameters.

D. Clock, elapsed time, or other event references.

Service routines will be provided to accomplish subfunctions of resource management described below. Requests for services, actions taken, and statistics relating to performance are recorded in the system log as instructed by flags in the system control table.

A. Permanent Queues—Will be implemented similar to temporary queues except where the function is well-defined and requires high efficiency. An example could be the queue for dispatching of a CPU to the next task to be executed. Queues such as the system log will appear permanent to an application program, but may be temporary with respect to the executive. Other system queues defined and maintained by the executive include:

   1. Main memory allocation.
   2. Auxiliary memory allocation.
   3. System log.
   4. System messages.
   5. Cyclic initiation.
   6. Elapsed time interval.
   7. Orbit or mission time reference.

B. Primary Support Subfunctions—Will reference allocation queues or control blocks and permit application or executive tasks to:

   1. Acquire—Control of standard size blocks of main or auxiliary memory. The size will be a function of the main storage protection mechanism or conventiently addressable auxiliary memory areas. Access to auxiliary memory will always be controlled by an I/O management function based on allocation information in the system auxiliary memory control block.
   2. Drop—Control of specified block or blocks currently controlled by the requesting tasks. Any information contained within the blocks will no longer be available.

3. Pass—Exclusive or shared control of specified block or blocks currently controlled by the requesting task to a specified program by means of the system communication function. Exclusive control or ownership is always unique to a particular program executing as a task or eligible to become a task. Shared control will be verified through use of the owner's identification or name and testing the identification and current control block status with respect to shared resource control logic.

C. Temporary Queues—May be defined in memory blocks assigned to the executive or the requesting application task. In either case, the same basic function is accomplished with re-entrant routines. But queues defined in executive blocks contain only basic control information and a limited amount of optional data specified with the request. Queues defined in memory owned by a requesting task will allow elements to be added or removed with optional data length fixed with the queue definition request.

D. Executive Queue Support—Subfunctions are defined and utilized in conjunction with the wait and post functions of program management. A queue may be defined as having a binary chain to define simplex or parallel control entries. The major subfunctions are:

1. Enqueue—Which requests that an element be added to the specified or named queue if it currently exists; otherwise, define the queue and then add the entry. The request may be to test status; define if required, and add an entry; add only if a queue is not built. The optional data specifies the queue name and simplex or parallel control branch. If an entry is made, control is optionally returned to the task unit controlling position of the queue is acquired. The service order will be by priority or FIFO with exclusive-request selected before shared requests.

2. Dequeue— Will remove an entry from the specified queue regardless of the chain position as long as it references the requesting task.

E. Application Queue Support Functions—Are defined and utilized in conjunction with the wait and post functions of program management. The function is used implicitly with the auxiliary memory access method of I/O management. The queue entries may be placed in main or auxiliary memory but top level control information will normally be in main memory. The implementation will include at least the following subfunctions:

1. Define—A main or auxiliary memory queue with entries to be limited to the length and number specified. Multiple tasks may reference the queue but only if the name and identification of the defining task is known.
2. Put—To add an entry to the queue. If auxiliary memory is utilized, the request is satisfied with supporting function of I/O management.
3. Get—To remove or read an entry of the queue. Removal permits reuse of the memory without redefining the queue. As with the Put subfunction, I/O management is required if auxiliary memory is involved.
4. Remove—All entries from the specified queue or remove the definition which prohibits further reference until redefined.

A.3.1.2.4 Input/Output Management

An input/output interface program will be included that provides a capability to permit concurrent development of many application programs and isolate software development from hardware development or changes to a significant extent. The interface will at least permit support software to be utilized for program instruction generation without explicit knowledge of physical device addresses or intersubsystem data flow paths and while the program is executing, knowledge of current input/output activity of other programs. Any exception or requirement of such knowledge should be handled either by utilizing executive queueing facilities or by taking advantage of hardware characteristics.

The program requesting services must provide its own buffer control processing. The buffer and I/O control above the basic access routine may be in the form of a shared support program for one or more application programs. The queueing logic of resource management is an example of shared support and may be used by application programs. The request for service may involve a single terminal poll operation or multiple operations in the form of chain of requests.

A. Request Handling—Determines the status of the units and queues associated with the request signals, abnormal condition to program management or the requestor, and normally chains the request for subsequent processing by the initiation function. The requests may involve data transfer to or from remote units or the monitoring to detect changes in remote data sources for posting of control blocks (≤ 31 total).

B. Initiation—Involves merging of outstanding requests that must be accomplished at the current or next available time period. Separate sequences are built for each data bus channel from periodic and aperiodic request queues.

C. Completion Processing—To signal an application program that a specific request has been satisfied, pass status information relating to the request.

D. Auxiliary Memory Access Routine—To allocate or release space and accomplish read and write operations for executive or applications programs. Main memory requirements will be reduced for processing functions or for communication among programs. The space may be shared by more than one program or program tasks, but requests are always for fixed length read or write operations (≤ 4096 words) either sequentially or by relative position in the allocated space.

E. Bulk Memory Access Routine—Shall provide control similar to auxiliary memory support but only for sequential reading and writing logical sets of data corresponding to a particular subsystem or task.

A.3.1.2.4.1 Input to I/O Management

Input in the form of requests to accomplish periodic or aperiodic polling of data bus terminals or units attached to such terminals. All requests are associated with a task control block and a corresponding program control block. The following information sources are also utilized.

A. System control table.

B. Task control table (and blocks as required).

C. Resource control table (and blocks as required).

D. I/O periodic request queue (and blocks as required).

E. I/O aperiodic request queue.

A.3.1.2.4.2 Output of I/O Management

Outpurs consist of signals to program management, information placed in output parameters or variables associated with individual requests, and possible updates to:

A. Task control block (requestor).

B. Resource control blocks.

C. System control table.

D. System log.

A.3.1.2.4.3 Processing

Requests for I/O related processing will be accepted from application or executive tasks. The requesting task must provide data buffers. Multiple requests may be outstanding for a task and execution of a task may be delayed at any subsequent time by issuing a wait request to the executive. Each request is associated with a particular task, resource, and event control block.

A. Request Handling—Provides an interface to permit program tasks executing concurrently on a multiprocessor or with interleaved segments on a simplex processor to effectively share communication channels and units. The function will provide a high level of abnormal interference protection among program tasks by validating requests against executive defined or monitored variables or control blocks. The major subfunctions will be:

   1. Open—Will be required to build or precondition a system resource control block to permit and verify individual program task requests with respect to communication channels or units and areas of main or auxiliary memory.

2. Close—Will be required before task termination to verify normal completion of related processing function and release or pass responsibility of system resources.
3. Start—Which references an individual or chain of individual read or write commands and a specific system resource control block. Integrity checks are made before the request is placed in the aperiodic request queue. Each request is associated with a system queue control block which links the request to the program task and permits asynchronous task execution unless a wait is also requested by the task.
4. Poll—Is similar to a start except the request is placed in the periodic request queue. The queue is organized and merged with the aperiodic request queue to satisfy different sample intervals for individual tasks, even though usage of communication channels and units may coincide. Program execution may be independent of periodic I/O but poll request options will permit posting or initiation when data is received or if a change has occurred to a discrete or analog limit check included in a current poll request.
5. Stop—Is issued by the program task to remove a previous poll request from the periodic request queue. If a task terminates, checks are made to insure that poll requests are not currently queued.

B. I/O Initiation—Is entered as a periodic program, directly from the request handling or other executive action such as I/O completion processing. Requests are checked to determine if the requesting task is permitted to enter a particular queue. Certain queues are designated for more request monitoring, thus permitting a program hierarchy to be defined within the executive or support programs for more efficient control of storage protect keys or shared devices and paths.

C. I/O Request Merging—Of requests will accomplish optimization of data bus and auxiliary memory communication consistent with the priority/precedent relationship that exists among the requesting tasks. The result of the merge operation is a chained sequence of read (command) and write (response) instruction for an I/O channel. The unit is directed to process the chain, store status, and signal the processor upon completion. The status is checked and appropriate output generated prior to initiating additional action on the particular channel.

D. I/O Completion Processing—Will analyze the status flags that were stored in main memory by the preceding chain of commands issued on a particular input/output controller channel. For normal status conditions, associated system event control blocks are posted and I/O initiation may be re-entered. Abnormal status is handled by a request retry routine unless inhibited by a flag in the system resource control block in which case the abnormal status is placed in the system event control block and the request is posted as complete.

E. Auxiliary Memory Access—Is used to read or write fixed length data blocks or segments of data blocks either sequentially or by specifying the relative data position. The routine may be utilized to read or write preassigned auxiliary data blocks as long as the data identification and owning program or program task are known. New data blocks can be named and assigned until the maximum block threshold is reached for the requesting task.

Usage can be exclusive or shared with other tasks as defined under request handling subfunctions.

F. Auxiliary or Bulk Memory Access—The access routine maintains the auxiliary memory control parameters with respect to the tasks that have issued an open request. The memory unit control commands are generated to provide standard recovery or retry sequences, integrity of individual program data, and efficient utilization respecting a limit number (TBD) of priority levels.

A.3.1.3 Data Base Requirement

The following paragraph specifies the data items that are an integral part of the executive or items which may be contained within application programs but referenced by the executive. The contents of other main or auxiliary memory data items are not important unless they indirectly relate to resource allocation or resource recovery, reconfiguration or program relocation, checkpointing, or other subfunction of the executive.

The data required for the executive may be satisfied by contents of auxiliary memory or by direct input from a central controlling processor. Except for the auxiliary memory and the description of the activity schedule, the data base requirements hold for a distributed processor but to a more limited level. Bulk memory requirements are TBD.

A.3.1.3.1 Auxiliary Memory

The first data locations of each auxiliary memory unit shall contain an initialization routine. This routine will contain instructions and data required to load and activate the primary executive, displays and controls, and communication programs. The preceding programs and data shall provide sufficient capability to control the subsequent system initialization processing including the updating of main or auxiliary memory locations under external control. For normal updating, other memory contents are described by a dictionary which follows the primary routines on each unit.

A.3.1.3.1.1 Initialization Routine

The routine will be made up of instructions and data sufficient to establish the preferential storage area and force the processor to load the primary programs. The data and logic are organized to inhibit all interrupts except those directly associated with the auxiliary memory transfer and hardware failure detection logic of units accomplishing the load and initialization function.

A.3.1.3.1.2 Primary Programs

Primary programs and data are located in fixed auxiliary memory locations identified in the initialization routine. The data contains information to replace the current contents of preferential storage areas and any information required to initialize the following main memory data areas to a state that will support external communication to the primary executive function:

A. System control table.
B. Program control table (and blocks as required).
C. Task control table (and blocks as required).
D. Resource control table (and blocks as required).
E. Cyclic initiation queue.

A.3.1.3.1.3 Auxiliary Memory Index

An index will be maintained to all locations and queues defined in the executive or areas assigned to any program. The entries shall contain at least the following information to describe auxiliary memory usage:

A. Responsible program.
B. Space allocated.
C. Physical location.
D. Current status.
E. Access history.

A.3.1.3.1.4 Other Allocations

Additional usage of auxiliary memory will be tailored to the capabilities selected for the particular Modular Space Station processor by ground support and will depend on the dynamic state of the on-board programs. The activity schedule table will be included if the processor is not to receive all task assignments from an external interface.

The following, as well as additional items, may have space allocated depending on the processor responsibilities.

A. Program library.
B. System log.
C. System messages.
D. Checkpoints.
E. Activity schedule.

A.3.1.3.2 Control Tables or Blocks

The exact data structure and data items beyond the preferential storage area (PSA) will be determined in subsequent design efforts. But the following subparagraphs present basic guidelines and describe a structure and lists data items consistent with system objectives, operational requirements, and design requirements presented in other paragraphs of the document. Permissible values for the data items and the internal audit checks will be established during detail design.

The system-level data structure is shown in Figure A-2 along with the relationship to physical DMS units. The subparagraphs describing the data structure are organized by major Executive management function.

A.3.1.3.2.1 System Management

System level control of DMS processing is maintained by the CPU hardware and microprogrammed logic utilizing data in scratch-pad memory (SPM) and main memory preferential storage areas (SPS) assigned to each CPU. The initiation sequence loads the initial load routine and data in the PSA assigned to the controlling CPU during system initialization. All PSA's are preset by the initial load routine following the loading of primary DMS programs and subsequent to passing control to the executive program contained in the set of primary programs. Every PSA of a processor will point to a single system control table which references addition data required for the primary progr ım set. Each PSA will contain at least the following information with replication as required by the current CPU assignments:

A. Scratch-pad memory refresh or checkpoint data.
B. Interrupt control data and program pointers.
C. Input/output and memory unit assignments.
D. Channel control data and program pointers.
E. CPU identification and alternate PSA pointer.
F. Current contents of address translate unit.
G. Current contents of configuration state unit.
H. Pointer to the system control table.
I. Currently assigned task control block.

A.3.1.3.2.1.1 System Control Table

The primary control information for the executive program will be contained in contiguous main memory locations to minimize problems of

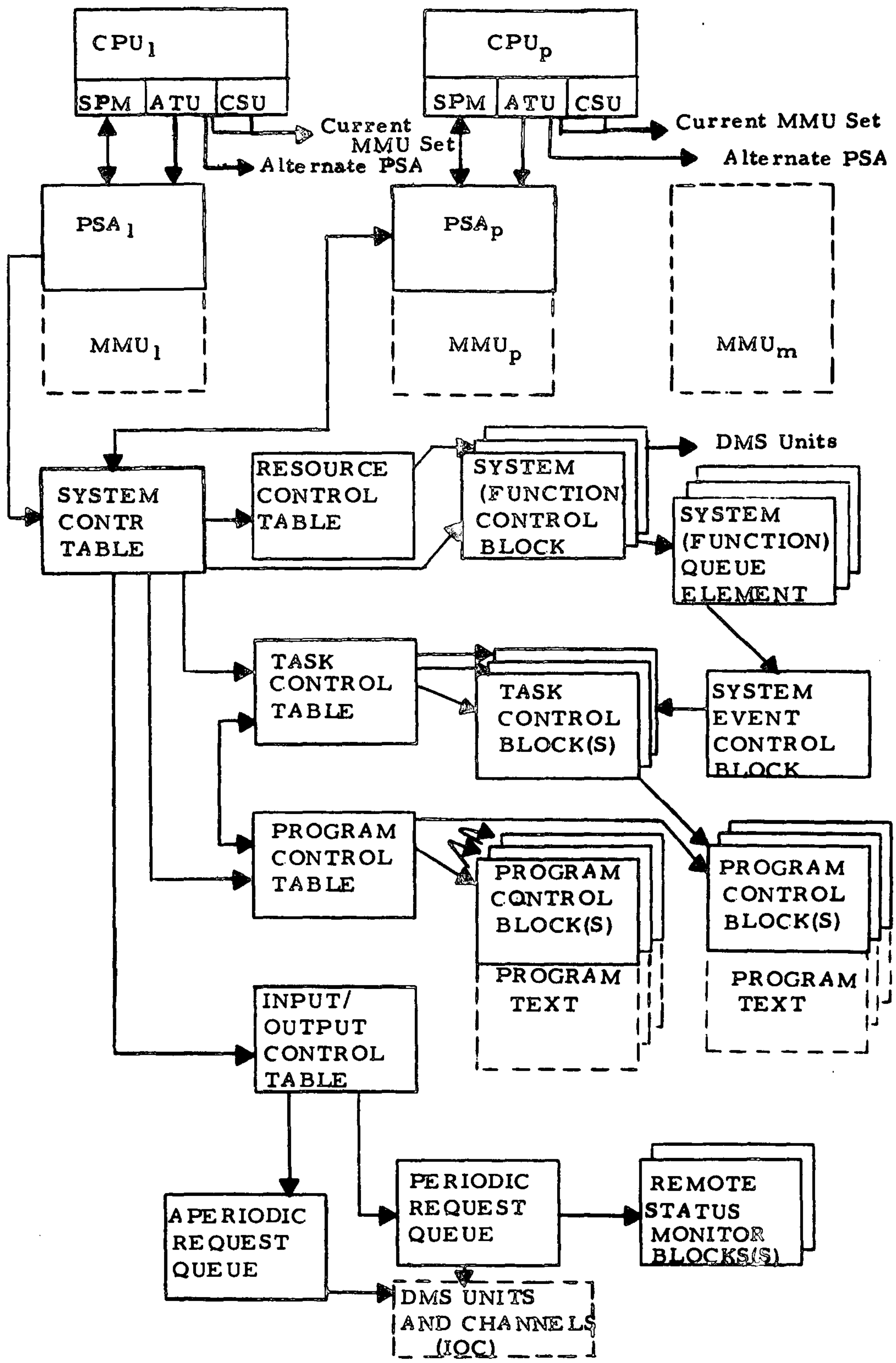


Figure A-2. System Level Data Structure

base register assignments. The table shall be organized in two parts corresponding to the constants and variables required by system management functions. Variable length data with respect to program generation or operational processing may be referenced by data items in the system control table (SCT) and stored noncontiguously as scattered blocks of data or stored as additional tables. SCT may contain the following items of information or additional key system information:

A. Packed reference data for tagging (date, time, orbit parameters, etc.).
B. Processor configuration data and unit status (CPU, IOC, MMU, and auxiliary memory).
C. System management control data (system queue control blocks, etc.).
D. Common support control data (checkpoint or log control flags, etc.).
E. Pointers to system control blocks.
F. Pointers to other executive tables.

A.3.1.3.2.1.2 System (Function) Control Blocks

The individual formats and data contents as well as the number of each type will be determined during program generation to tailor the executive program to the requirements of the particular processor. To a limited extent, this definition may be modified by the system reconfiguration routine. Control blocks will be defined for in at least the following areas:

A. CPU dispatching
B. Reconfiguration requests.
C. Log queue and request control.
D. Checkpoint queue and request control.
E. Messages queue and request control.
F. Message routing.
G. Interval timer control.
H. Real-time clock control.
I. Elapsed time or real-time signal request queueing.

The highest level control block for a particular resource may contain constants established during program implementation or system generation. Optional fields may be included during program implementation and be checkpointing, logging, or executive function control logic. The information contained may include but not be limited to:

A. Current status and priority.

B. Unique identification.

C. Program control block reference.

D. Task control block reference.

E. Normal termination count.

F. Abnormal termination count.

G. Control flags for log or measurement functions.

H. Optional measurement variables.

As with the task control table, the contents will depend on the display and real-time control requirements but each entry shall not exceed eight 32-bit words.

A.3.1.3.2.2.4 Task Control Block

Additional temporary display and control information relating to a task shall be in a unique task control block, but shall remain defined only for the time between initiation and termination of the corresponding task. The control information shall only be the information required to maintain a single-thread processing sequence and not more than one additional level of executive program control relating to asychronous events. Microprogrammed interrupts or internal processing traps may require two levels. Information may include but not be limited to:

A. Normal processing initiation reference.

B. Processing restart reference point.

C. Current status.

D. Task control table reference.

E. Register save areas (≤two levels).

F. Current location (≤two levels, processing suspended).

G. Parent task reference.

H. Offspring task reference.

I. Resource allocation thresholds.

J. Current resource holdings (or references).

selected while generating the executive program for a particular processor. The purpose is to select system debug or monitor and data recording functions. Data recording may be in preassigned variable fields or the system log. Each subordinate control block shall contain only basic variable parameters relating to the function and the identification of the requesting or responsible task.

A.3.1.3.2.2 Program Management

Program Management functions utilize two basic control block structures corresponding to main memory content and processing sequence control. The program control table contains constants and variables utilized by routines to initiate, terminate, or provide support functions to on-board programs. During processor operation, the table contains pointers to the currently loaded program modules and corresponding program control blocks. For those program modules with prime processing responsibility within an application, additional priviledges or services are provided. The control constants and variables for the latter will be referred to as 'task' rather than 'program'.

A.3.1.3.2.2.1 Program Control Table

Program modules that are currently resident in main memory will have location references and current status maintained in the program control table. Any frequently used program module shall be included, even though it may not be currently resident and the location reference will indicate the auxiliary memory location or the remote processor responsible for supplying the module. Other information may include but not be limited to:

A. Sharable module status.
B. Module size.
C. Immediate reuse probability.
D. Normal exit count.
E. Abnormal exit count.
F. Program or task control block pointer.
G. Module text pointer.

The selection of information for individual programs will be determined by the DMS status display requirements and the real-time program control algorithms implemented and shall not exceed four words.

A.3.1.3.2.2.2 Program Control Block

Every program module will be stored in auxiliary memory during any execution cycle to simplify restart and recovery procedures even though the program may be normally stored in bulk memory or in a ground-support facility. Frequently used programs will remain in auxiliary memory to reduce loading overhead and complexity and to reduce the delays that would result from immediate initiation demands. Every program or program module will be described by information contained in a program control block, and the block will reside with the module regardless of current placement in the memory hierarchy.

The program control block will contain a fixed-length basic section for all modules, which will contain at least the following type of information.

A. Unique module identification.
B. Program name or code.
C. Module size.
D. Module characteristic flags.

Modules that are eligible for initiation as a task will have additional information in an extension area of the program control block. The extension area will always have the same organization but because resources requirements may vary, the block length may be different for different modules. The extension area will at least contain the following type of information:

A. Execution priority and entry references.
B. Internal instruction and/or data references.
C. External instruction and/or data requirements.
D. Resource requirements and utilization limits.

A.3.1.3.2.2.3 Task Control Table

Every program module eligible for initiation as a program task will have current status reflected in the task control table for display to the crew, A.3.1.3.2.3 Resource Management

Resource management is responsible for maintaining control information describing currently available DMS resources, resource allocation criteria, and resources currently assigned to the executive or application programs. While a resource is allocated, the control information shall identify the resource and the task or tasks utilizing the resource. In addition, optional resource utilization flags will be maintained to control log or monitor functions.

A.3.1.3.2.3.1 Resource Control Table

Common constants and variables relating to resource monitoring and control will be maintained in the resource control table to simplify display, checkpointing, monitoring, and allocation or deallocation processing logic. The table shall either contain or reference system queues defined or utilized by any executive function.

A.3.1.3.2.3.2 Resource Control Blocks

Control blocks shall be defined to control the use of DMS resources but every attempt shall be made to minimize the unique formats required. Unique control blocks will be required for processor and memory allocation to minimize processing overhead.

A.3.1.3.2.3.3 Queue Control Block

Main or auxiliary memory storage areas allocated to a task and identified as a single logical set will be controlled as a single unit by the executive data defining or used to control the logical set maintained in a queue control block. The queue control block may contain but not be limited to the following information:

A. Unique queue identification.
B. Response task reference.
C. Currently allocated storage blocks.
D. Allocated storage block limit.
E. Multiple-task access control flags.
F. Responsibility reassignment control flags.
G. Current status.

The executive program shall include the following permanent or dynamically defined system queues and associated control blocks:

A. Program library.

B. Activity schedule (access only).

C. System log.

D. System messages.

E. Checkpoints.

Any system queue that is expected to increase in size beyond a level acceptable (TBD) to have resident in main memory or which must be duplicated for system integrity shall be assigned to auxiliary memory.

A.3.1.3.2.4 Input/Output Management

Except for remote status monitoring, all data bus input and output will be accomplished by specific communication control commands defined by an application program. The executive program will be responsible for device and channel addresses, validating requests to insure system integrity, merging sequences of control commands, initiating IOC processing of merged sequences, and postprocessing of completed sequences. Control commands by application programs references shall be supported by application units attached to data bus terminals or discrete or analog line serviced by remote data acquisition/distribution units. The references are always symbolic designation and the actual address is established by support programs and the executive program. Access to auxiliary or bulk memory will always utilize routine and control blocks defined by the I/O management routines.

A.3.1.3.2.4.1 Input/Output Control Table

The physical unit and channel addresses and current status will be maintained in the input/output control table or in associated control blocks (TBD). The information may include but not be limited to:

A. Symbolic identification.

B. Unique unit identification.

C. Current channel assignment.

D. Current status.

E. Reference to responsible task.

F. Reference to aperiodic request queues.

G. Reference to periodic request queues.

H. Remote status monitor control data.

I. Auxiliary or bulk memory access control data.

J. Control flags for log and measurement functions.

K. Optional measurement variables.

A.3.1.3.2.4.2 Aperiodic Request Queues

Any program may request (START) input from or output to remote units by preparing one or more communication control blocks. The blocks will contain data bus command words and command data or references to response data area assigned to the requesting task. Data bus channel references will not be permanently assigned but are preupdated based on information contained in the input/output control table. The executive program shall signal requesting programs on the first request subsequent to a channel address switch.

Input/output management will maintain a set of unordered queue elements and as time becomes available on the required channel, the elements will be merged to a single communication sequence and passed to the input/output control unit servicing the channel. Each request element will contain at least the following information:

A. Task control block reference.

B. System event control block reference.

C. Communication control block reference.

D. Predicted channel time.

E. Channel reference.

A.3.1.3.2.4.3 Periodic Request Queues

Periodic data bus communication will be requested similar to aperiodic, except that the executive program will maintain the queue elements following a merge operation. Once a task has requested periodic communication (POLL), the elements are retained until the task terminates or a request is received from the task (STOP). The queue elements contain the same information as with the aperiodic requests and the following information.

A. Poll time interval.

B. Time reference requirement (or acceptable delay).

A.3.1.4.2.4.4 Remote Status Monitor Blocks

Control information shall be maintained by input/output management standard control of remote units and additionally, permit applications to request or cancel requests for posting of system event control blocks (SECB) when a referenced condition changes. One or more discrete conditions shall be mapped to a single SECB. The data structure may correspond to the "Reference to responsible task" contained in the input/output control table. The monitor set may be less than the "responsibility set" and therefore monitor mask flags shall be provided. The discrete conditions may include out-of-limit analog conditions as well as changes in a particular discrete signal line. The information maintained shall include:

A. Monitor mask.

B. Monitor interval by task (by task or SECB).

C. Reference status.

D. Task reference.

E. Analog input limit check.

F. Analog output gain setting.

G. Current status.

A.3.1.4.2.4.5 Auxiliary Memory Access

Control blocks shall be defined sufficient to interface with resource management functions and permit access to auxiliary memory areas by TBD tasks concurrently. The control data will be sufficient for programmed control logic to insure the security and the integrity of stored data to the task level. Auxiliary memory space shall be definable as discrete areas with access permitted for reading or writing by tasks on a shared or exclusive basis. Basic control information for each area will be maintained in blocks as defined for auxiliary memory queues in resource management.

A.3.1.4.2.4.6 Bulk Memory Access

A subset of the control blocks required by the auxiliary memory access routine will be utilized to support sequential read or write of bulk memory.

A.3.1.4 Human Performance

The executive program organization permits operation of DMS in manned and unmanned phases of Modular Space Station buildup. During manned operation, the direct interface requirements for the crew shall be limited to forcing system initialization, reconfiguration, or termination. The latter two and at least the following crew control and monitor actions shall be permitted through an executive, displays and controls; or a communications subsystem interface.

A. Output current DMS configuration status.
B. Output current application program status.
C. Output current DMS utilization levels.
D. Change current DMS configuration.
E. Change current application program status.
F. Change current system control table parameter.

Preliminary validation and crew or ground communication processing is the responsibility of the particular subsystem. The executive program processing is limited to final checking of configuration change requests in order to ensure integrity of the system and the actual accomplishement of the changes. Other crew actions will be defined for DMS but will not directly affect the executive.

A.3.2 <u>CPCEI Definition</u>

The following subparagraphs specify the functional relationships of the executive program to other on-board programs and hardware. Government-furnished items relating to program development or operational processing will be identified.

A.3.2.1 Interface Requirements

The interface to application programs and the executive program will be limited to communication data in main memory in the form of well defined and monitored data blocks. Requests and response to requests by the executive will occur in conjunction with the processor switching between the non-priviledged and priviledged mode of executing instructions in a simplex processor. In a multiprocessor, the requests and responses may be controlled by well-defined queues and lock indicator manipulated by a test indicator, set, and skip type instruction.

A significant portion of the time required for execution sequence or task switching can be reduced by register replication in the SUMC. Additional time can be reduced by microprogramming portions of task switching, I/O request merging, and I/O completion processing.

A.3.2.1.1 Interface Block Diagram

Figure A-3 is a system level flow depicting the relationship among the major subsystems. The following paragraph presents a more detailed description of the control and data flow between the executive functions and external interfaces.

A.3.2.1.2 Detailed Program Interface Description

All application programs with the exceptions of displays and controls, DMS maintenance, and certain communications programs utilize a standard communication interface with the executive. The exceptions require more complex data blocks for communication and significantly more parameter testing is required to insure a high level of system reliability. The interface will always utilize the standard priviledged and non-priviledged processor modes except for well verified DMS maintenance routines and then only for subfunctions requiring priviledged instructions.

A.3.2.1.2.1 Program Generation and Documentation

Each application program is a set of one or more elements or program modules each of which are described by a program control block. The control block is made up of a fixed portion and a variable portion. The fixed portion includes the module identification, the size, and characteristic flags. Flags are at least included to describe the following characteristics:

A. Instructions or data.
B. Re-entrant instructions or data constants.
C. Task status eligibility.

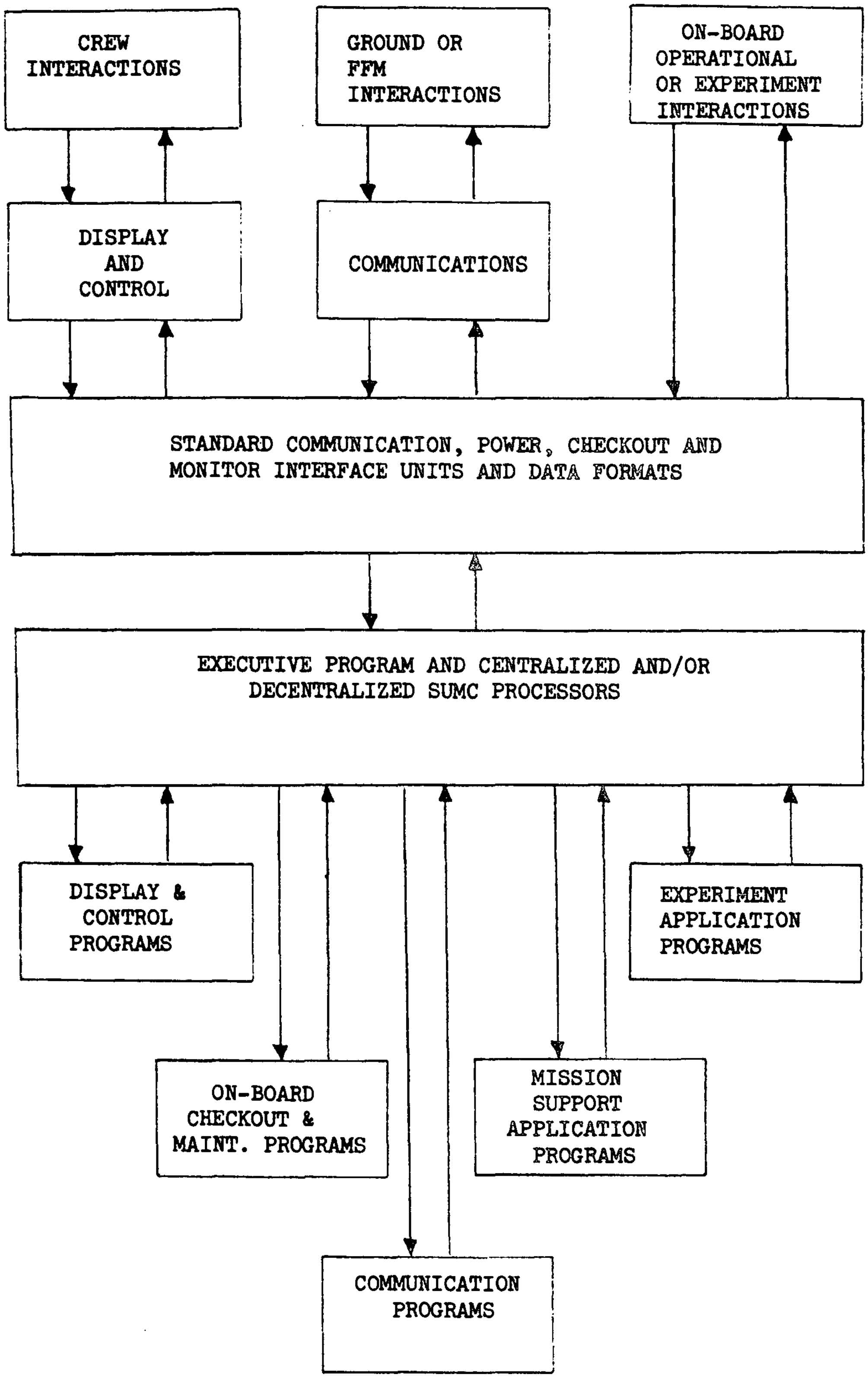


Figure A-3. Software/Subsystem Interfaces

Appendix B

DATA BUS SYSTEM SPECIFICATION FOR THE MODULAR SPACE STATION DATA MANAGEMENT SUBSYSTEM

B.1 SCOPE

This specification defines the data bus design and performance requirements for the Modular Space Station data management subsystem.

B.2 APPLICABLE DOCUMENTS

B.3 REQUIREMENTS

B.3.1 Data Bus Definition

The data bus for the Modular Space Station (MSS) shall provide for the distribution of analog and digital data throughout the MSS experiment and logistics modules when attached to the MSS. The data bus shall consist of the following assemblies:

A. Data bus terminals (DBT's).
B. Modems.
C. Remote data acquisition units (RDAU's).
D. Coaxial cable.
E. Coaxial cable couplers.
F. Coaxial cable terminations.
G. Shielded pair cables.

B.3.1.1 General Description

An overview of the total data distribution system for the MSS is shown in Figure B-1. A redundant bus is shown for both the analog and digital data buses. Redundant modems and terminals are provided for critical functions.

The analog data buses provide for audio and video transmissions directly on assigned frequency division multiplexed channels. The audio system utilizes

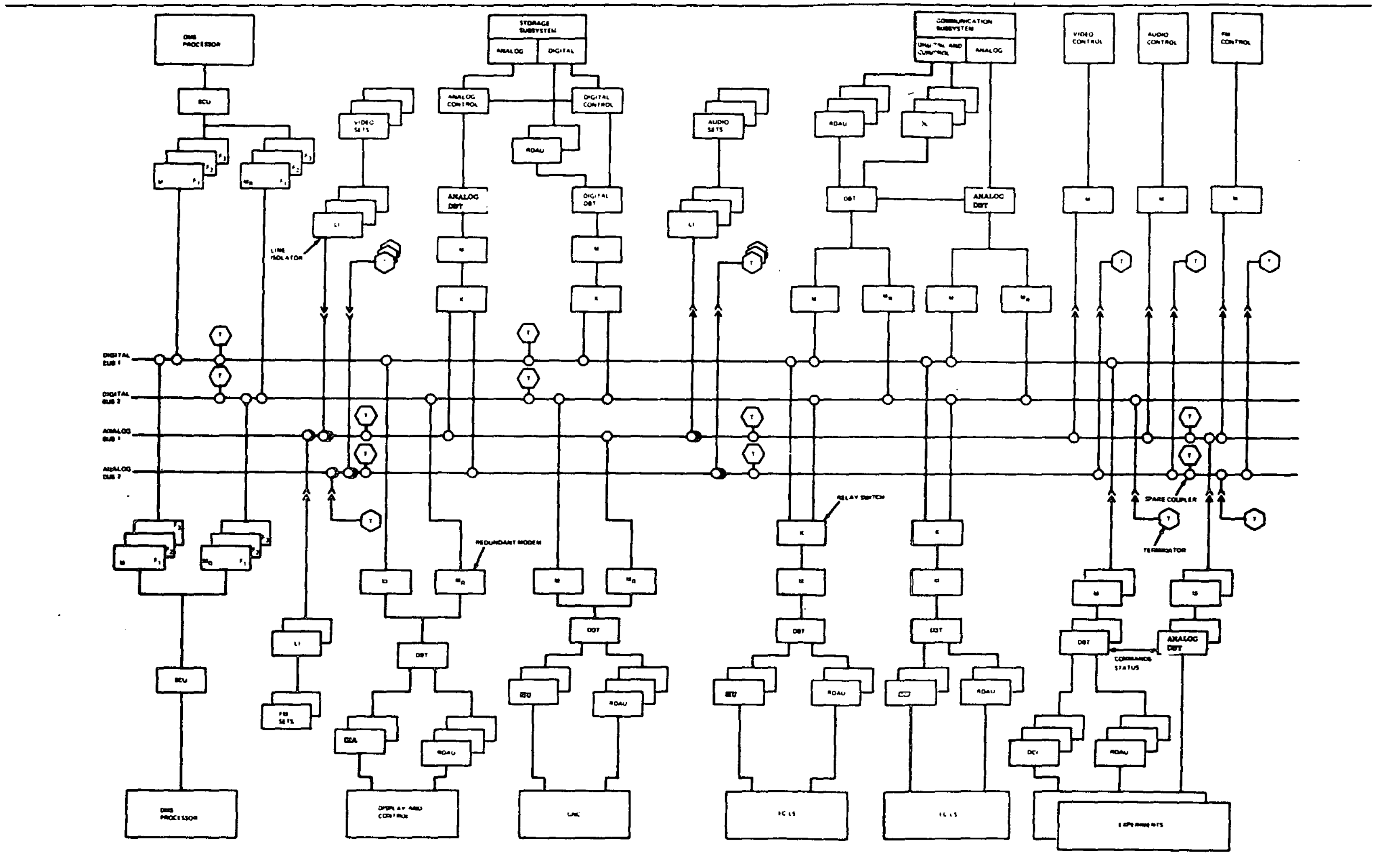


Figure B-1. Data Distribution Subsystem Design single sideband suppressed carrier and submultiplexing techniques to accommodate up to 48 audio channels. The video system utilizes standard CATV (cable television) techniques but employs a higher safety margin by using additional 2 MHz guardbands between video channels.

The digital data bus system contains three 10-MBPS FDM channels. The digital data bus operates under control of the input/output controller (a computing assembly) and interfaces with subsystem and experiment elements through digital data bus terminals, standard remote data acquisition units, and customized interface adapters considered to be parts of the subsystem or experiment serviced. The data rate between the DBT and each input/output device (RDAU or customized interface adapter) is 1 MBPS per channel.

B.3.1.2 Missions

The data bus in conjunction with the computing assemblies is used to support MSS subsystem and experiment operations during the 10-year operational orbital lifetime of the MSS.

B.3.1.3 Operational Concepts

B.3.1.3.1 Analog Data Distribution

The analog data bus shall distribute video and audio signals through dedicated FDM channels. Any receiver capable of being tuned to that channel can monitor all transmission in that channel. Thus, several video monitors may monitor the same transmission. The control of transmitting and receiving devices may be accomplished remotely and automatically where the device controls are connected to the digital data bus or where analog controls are connected to separate FDM channels interfacing with a command decode functional unit. Most controls, such as on-off switches, may be operated remotely through the use of the control functions of an RDAU on the digital data bus. However, it is anticipated that most of the analog system control will be accomplished manually. On-off functions may be handled remotely from the control stations, but such things as video receiver channel selectors shall be controlled manually, either with a rotary- or pushbutton-type channel selector switch.

The audio system shall contain an emergency voice channel at baseband with preempts all other audio channels and bypasses all on-off switches. In addition, three FM entertainment channels shall be provided on a 24-hour basis for astronauts off duty. Previously recorded analog magnetic tapes shall be selected according to channel and time.

Telephone channels shall be handled with standard telephone circuit techniques, except that no central switching unit is necessary with the channels. These channels shall provide enough capacity to carry all required station-to-station conversations, Space Station-to-ground calls, and conference calls requiring up to eight different stations tied in simultaneously.

B.3.1.3.2 Digital Data Distribution

The digital data distribution system shall transfer data by the use of an asynchronous TDM/FDM data bus. Three 10-MBPS digital channels shall be used in a command response operational mode to handle the generated data.

All digital operations on the data bus shall be controlled by the executive routine of the subsystem computing facility multiprocessor through its input/output controller (IOC). In the event of scheduled maintenance or emergency shutdown of this facility, bus control will be assumed by the experiment computing facility. Each device connected to the data bus shall be controlled by a data bus terminal (DBT) which serves as the interface between the data source and the data bus. One of three data bus channels shall be available to each DBT by the proper modem selection. A DBT shall contain up to three modems to allow different data channel selections.

Each terminal will be commanded by the control processor at preprogrammed intervals. These intervals may vary depending on the application and are adjustable by making modifications to the executive program. The most common interrogation intervals are 0.01, 0.1, 0.5, 1, and 10 seconds. Data bus terminal interfacing with subsystem devices such as RDAU's will be commanded at regular intervals depending on the measurement criticality.

B.3.2 Characteristics

B.3.2.1 Performance

The data bus for the Modular Space Station data management subsystem shall meet or exceed the requirements contained in the following subsections.

B.3.2.1.1 General

The data bus shall be capable of distributing audio, analog, video, and digital signals throughout the Modular Space Station and associated experiment modules when they are attached to the MSS. Channel allocations shall be in accordance with Figure B-2.

B.3.2.1.2 Emergency Channel

An emergency voice channel which preempts all other audio channels and bypasses all on-off switches shall be provided.

B.3.2.1.3 Telephone Channels

Forty-eight telephone channels, each having a bandpass from 300 to 3,000 Hz shall be provided. These shall be submultiplexed by SSB/SC/AM in the frequency range from 60 to 252 KHz and distributed with a minimum of 90 percent intelligibility. Audio channel performance requirements are indicated in Table B-1.

B.3.2.1.4 Entertainment Channels

Three entertainment channels shall be provided. These shall be frequency modulated onto carriers of 1.0, 1.15, and 1.3 MHz, with a bandwidth of 150 KHz centered about each carrier frequency.

B.3.2.1.5 Video Channels

Nine video channels shall be provided. Each video channel shall have a 6-MHz vestigial sideband AM bandwidth and a 2 MHz guardband. These shall be located at 8 MHz intervals beginning at 6.75 MHz and extending to 76.75 MHz with a minimum detected signal-to-noise ratio of 39 db. Video channel performance requirements are indicated in Table B-2.

(1) Public Address, Emergency Call, 300 to 3,000 Hz

(2) Telephone Carrier Reference, 4,000 Hz Sine Wave

(3) Emergency Call Tone, 5,000 Hz Sine Wave

(4) Emergency Alert Tone, 6,000 Hz Sine Wave

(5) 36 Telephone Channels, 60 KHz to 252 KHz, SSB-Sc-AM, 300 to 3,000 Hz Audio

(6) 3 Entertainment Channels, 1.0 MHz ±75 KHz, 1.15 MHz ±75 KHz, 1.3 MHz ±75 KHz, Frequency Modulated

(7) Television Carrier Reference, 4 MHz Sine Wave

(8) to (15) Television and Video Channels, 4.75 MHz Baseband, 6 MHz Vestigial Sideband AM, Carrier Frequencies Spaced at 8 MHz Intervals Starting with 8 MHz, 2 MHz Guard Band.

(16) Onboard Generated Test Channel, 4.75 MHz Baseband, 6 MHz Vestigial Sideband AM, Located in the Inter of 70.75 to 76.75 MHz.

(17) Digital Data Channels, 3 Only Shown 25 MHz per Channel.

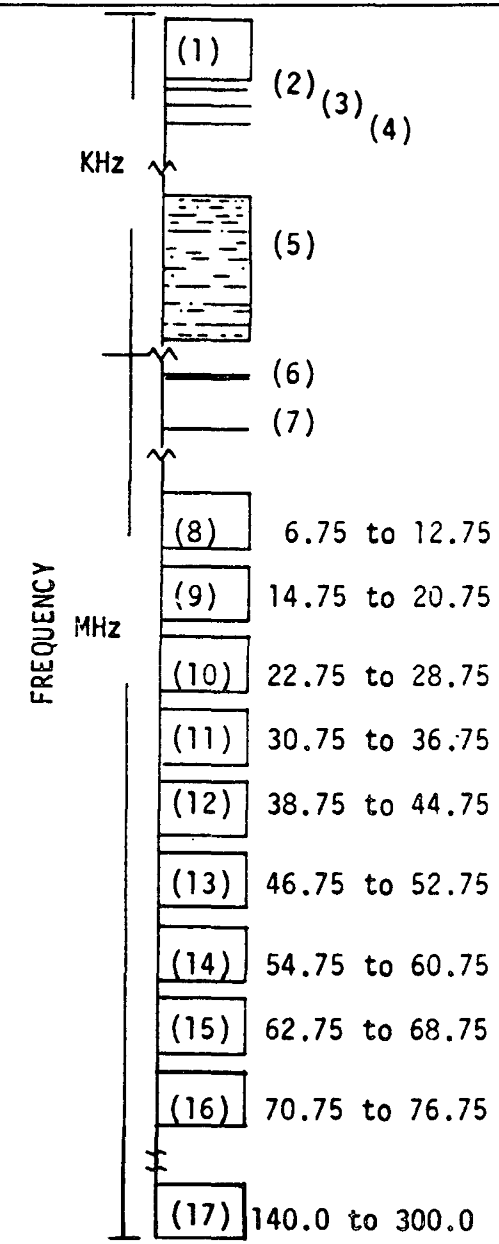


Figure B-2. Channel Allocation Chart

Table B-1

AUDIO CHANNEL PERFORMANCE REQUIREMENTS

Receiver	
Bandwidth:	3 KHz
Noise figure:	30 db
Dynamic range:	50 db
Sensitivity:	Minus 105 dbm with the specified bandwidth and noise figure at 20°C ambient temperature
Transmitter	
Bandwidth:	3 KHz
Modulation:	Single-sideband suppressed carrier
Unmodulated Carrier Power Output	21 dbm

Table B-2

VIDEO CHANNEL PERFORMANCE REQUIREMENTS

Receiver	
Bandwidth:	4.75 MHz (6 MHz vestigial)
Noise figure:	10 db
Dynamic range:	40 db
Sensitivity:	Minus 98 dbm with the specified bandwidth and noise figure at 20°C ambient temperature
Transmitter	
Unmodulated carrier power output:	28 dbm
Modulation:	Vestigial sideband
Bandwidth:	4.75 MHz (6 MHz vestigial)

B.3.2.1.6 Digital Data Channels

The data bus shall be capable of accommodating up to eight digital channels capable of distributing biphase signals at rates up to 10 MBPS, with bit errors less than one in 10^7 bits. Three channels shall be located in the frequency range of 140 to 300 MHz, with double sideband amplitude modulation techniques and a detected signal-to-noise ratio of at least 22 db.

Channels 1, 2, and 3 shall have center frequencies of 140, 210, and 300 MHz respectively. Digital performance requirements are indicated in Table B-3.

B.3.2.1.6.1 Message Formats

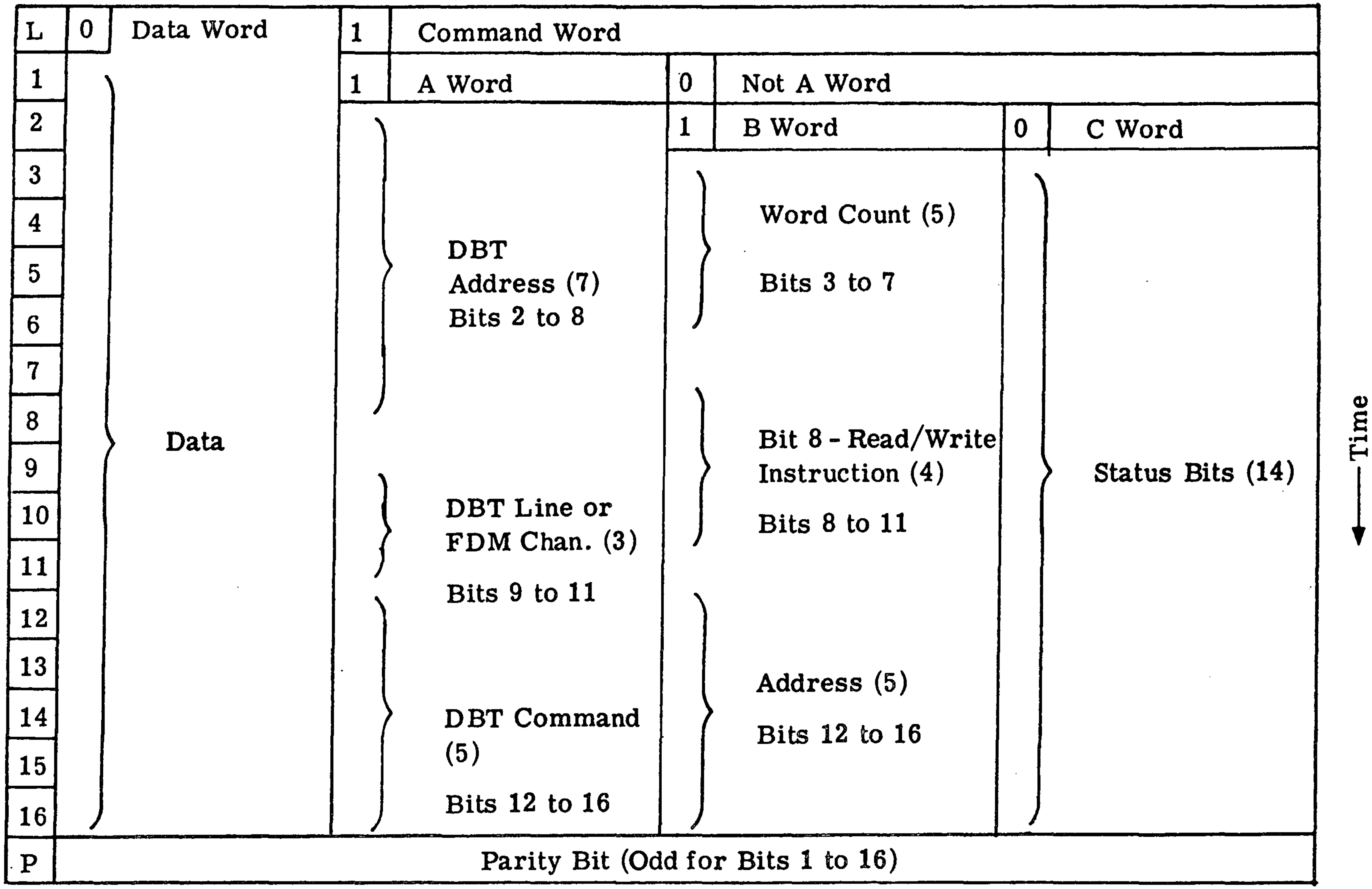
All communications or messages in data bus digital channels shall either be "commands" generated by the IOC or "responses" generated by one of the digital data bus terminals (DBT). These messages shall be transmitted in an ordered sequence and consist of a combination of 18-bit words.

The digital data bus shall accommodate the word formats shown in Figure B-3. Four types of 18-bit words are identified as "A," "B," "C," or "D" words. An "A" word contains the DBT address and command; a "B" word contains a word count, the device instruction, and the I/O channel address; a "C" word contains status; a "D" word contains data. Command messages occur in the form of an "A" word, followed by data if any, and ending with a "B" word. A normal response to a command consists of the echoed "A" word, followed by up to 32 data ("D") words, and ending with a "C" word. Each bus transmission starts with a synchronization burst followed by an "A" word, data if any, and ends with either a "B" or "C" word. In a device-to-device transfer, an additional A' and B' word are transmitted from the IOC to the DBT as two data words, i.e., having identical formats as an "A" and "B" word, but containing a lead zero rather than a lead one. This data provides the address of the second device and contains any necessary control information. The DBT then reinserts the lead ones and uses these data words as control words for device-to-device transmissions.

Table B-3

DIGITAL CHANNEL PERFORMANCE REQUIREMENTS

Receiver	
Data rate:	10 MBPS per channel
Data coding:	Manchester type II biphase Code format
RF bandwidth:	25 MHz ± 0.5 MHz per channel
Modulation:	Double-sideband amplitude modulation
Noise figure:	8 db
Sensitivity:	Minus 92 dbm with the specified bandwidth and noise figure at 20°C ambient temperature
Response delay:	2.3 microseconds maximum
Center frequency:	Channel 1 - 140 MHz Channel 2 - 210 MHz Channel 3 - 300 MHz
Signal-to-noise ratio:	22 db minimum
Bit error rate:	10^{-7} maximum
Transmitter	
Data rate:	10 MBPS per channel
Data coding:	Manchester type II biphase coding format
RF bandwidth:	25 MHz ± 0.1 MHz
Modulation:	Double-sideband amplitude modulation
Unmodulated carrier power output:	20 dbm
Turn-on delay:	400 nanoseconds maximum



L = Lead Bit
P = Parity Bit

Figure B-3. Data Bus Word Formats

B. 3. 2. 1. 6. 2 System Timing

Information transfer between data bus connected devices occur in the formats specified in paragraph B. 3. 2. 1. 6. 1. This paragraph describes the timing of each sequence.

Transfers between the IOC and DBT are illustrated in Figures B-4 and B-5. Figure B-4 shows the normal sequence for transfer of data from the DBT to the IOC (identified as a read mode). In a typical read sequence, the IOC transmits synch, an "A" word, and a "B" word to the DBT. This requires something less than 6 microseconds. In response, the DBT generates a synch burst, an echo "A" word, up to 32 16-data-bit plus 2-control-bit-data words, and ends with a "C" word containing terminal status information. This requires approximately 63 microseconds. The total response time (from time of command initiation to receipt of message) is approximately 73 microseconds with circuit and propagation delays accounting for approximately 4 microseconds. In the event special data is required from an I/O device such as a remote data acquisition unit (RDAU), a special request sequence must be serviced, whereby a large time delay of 738 microseconds is allowed for data transfer from an I/O device to the DBT at 1 MBPS. The IOC issues a command consisting of synch, an "A" word, and a "B" word. This requires approximately 6 microseconds. The DBT responds with a synch, an echoed "A" word, and a "C" word. This also requires approximately 6 microseconds. After a delay of 8 microseconds, the DBT transmits the "B" word to the I/O device (hereafter assumed to be an RDAU). This transfer requires approximately 19 microseconds. The RDAU responds within 4 to 14 microseconds with the data transfer taking up to 576 microseconds for a total elapsed time of approximately 638 microseconds, allowing for circuit and propagation delays. The typical read sequence is then initiated to bring data to the IOC. Total elapsed time will be less than 710 microseconds. The data bus channel is only occupied for 85 microseconds and other functions can be performed during the channel free time.

Figure B-5 illustrates the typical write mode. The IOC transmits a synch word, an "A" word, up to 32 18-bit data words, and a "B" word, requiring 63 microseconds. The DBT responds with a synch word; an echoed "A" word, and a "C" word. After a delay of 8 microseconds, a "B" word is

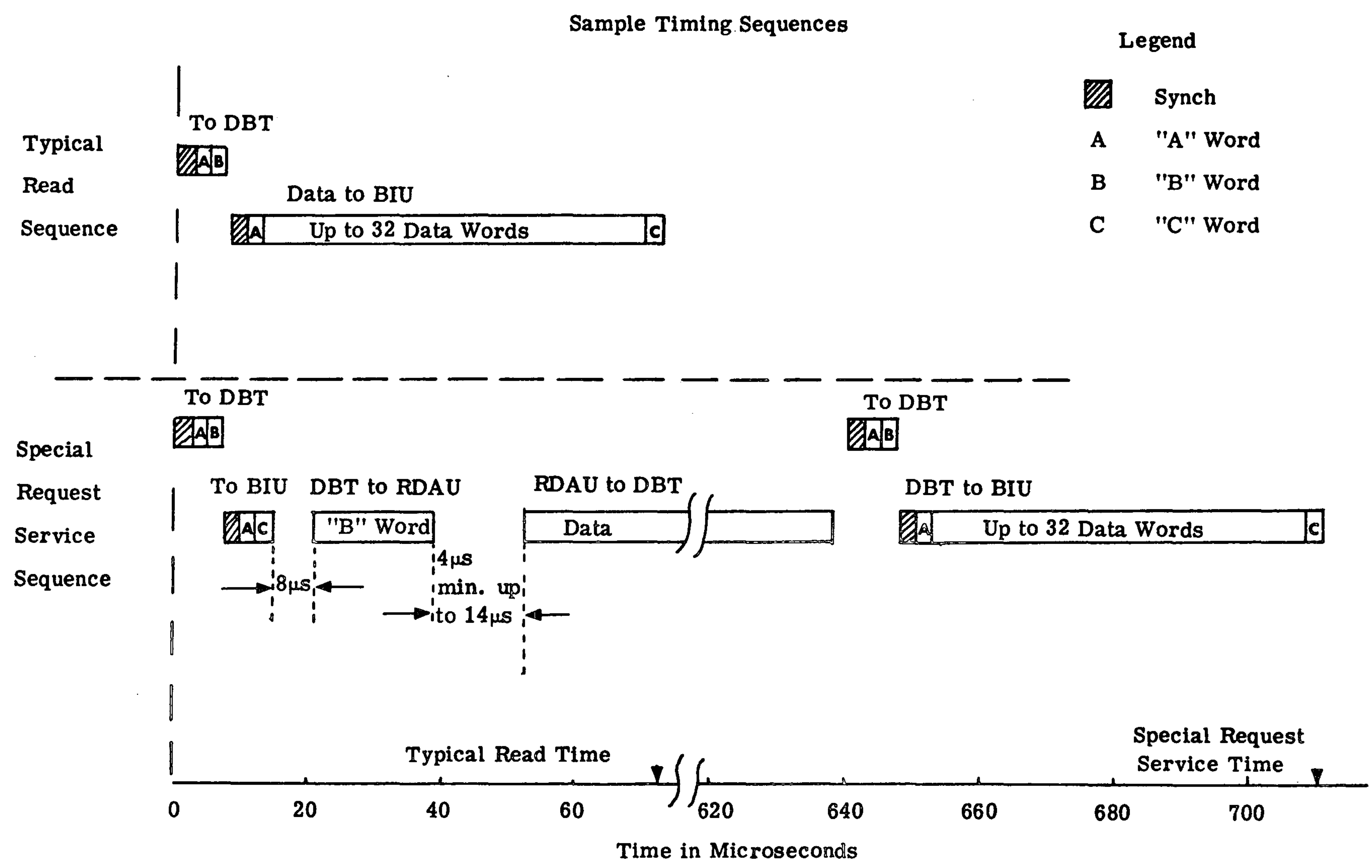


Figure B-4. Read Sequence Timing

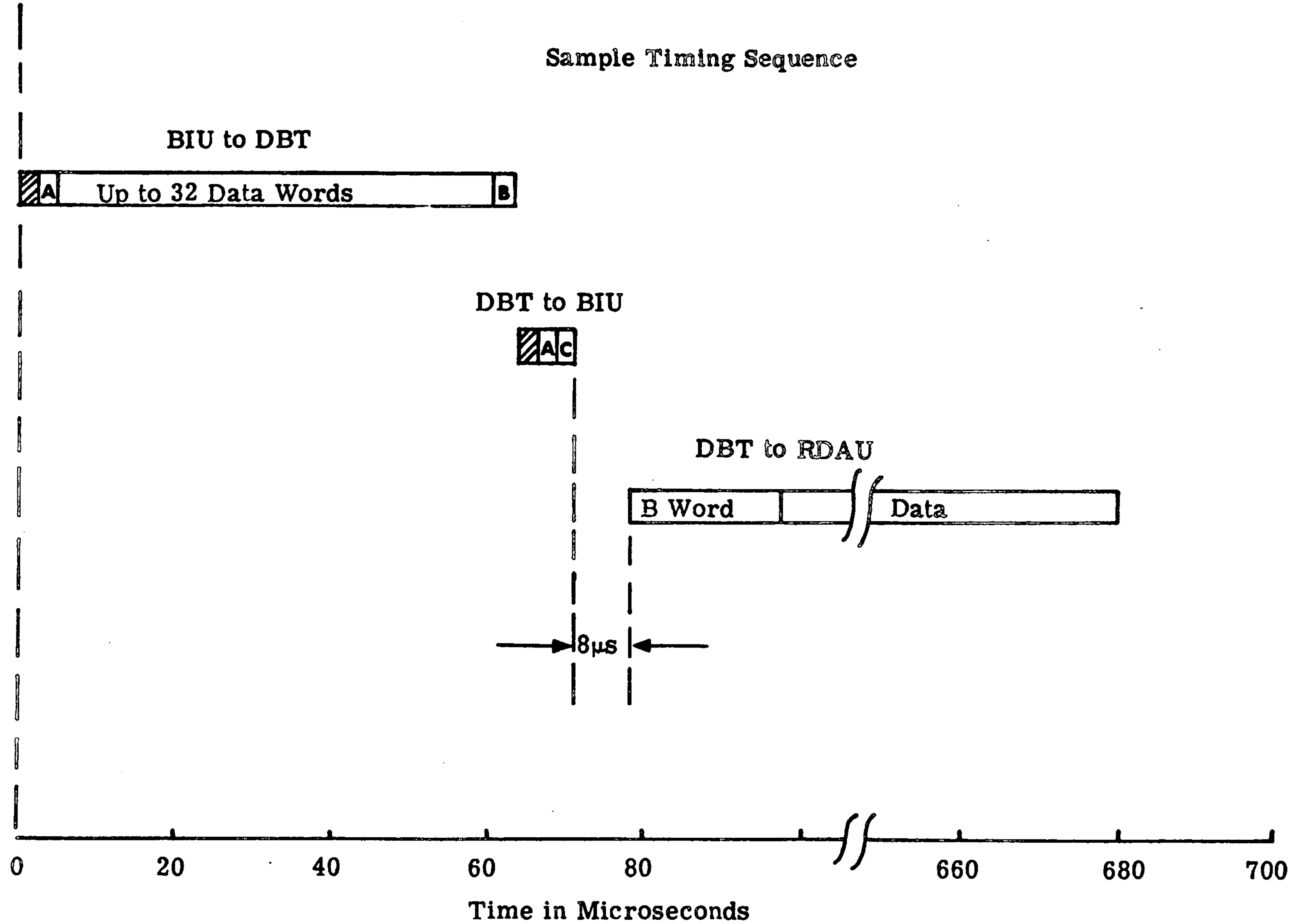


Figure B-5. Write Sequence Timing

transmitted to the RADU followed by up to 32 data words. Total elapsed time will be less than 680 microseconds. The data bus channel is only occupied for approximately 12 microseconds however, and can be utilized to perform other functions.

The sequence for terminal to terminal information transfer is shown in Figure B-6. In the event that both terminals are not on the same channel, a preliminary command must be sent to switch one of the terminals (identified by the address of the "A" word) to the other's frequency channel. This sequence is not shown in the figure. The IOC transmits a synch, an "A" word, and "A" data word, a "B" data word, and a "B" word. The DBT responds with a synch word; and "A" word, and a "C" word. After a nominal delay time (approximately 1 microsecond), the DBT transmits another synch word; an A' word, up to 32 18-bit data words, and a B' word. The DBT identified by the address field in the A; word receives the data and responds with a synch word; an echoed A' word, and a "C" word. This sequence is repeatable with A' and B' words issued with each terminal-to-terminal transfer sequence. The total sequence will require less than than 84 microseconds, but occupies the data bus channel for the full amount of time. Therefore, the data bus channel is occupied for the total length of time required for terminal-to-terminal transfer. The reset command is issued to the DBT identified by the "A" word to reset the FDM channel, if necessary, and to reset the registers containing the A' and B' words.

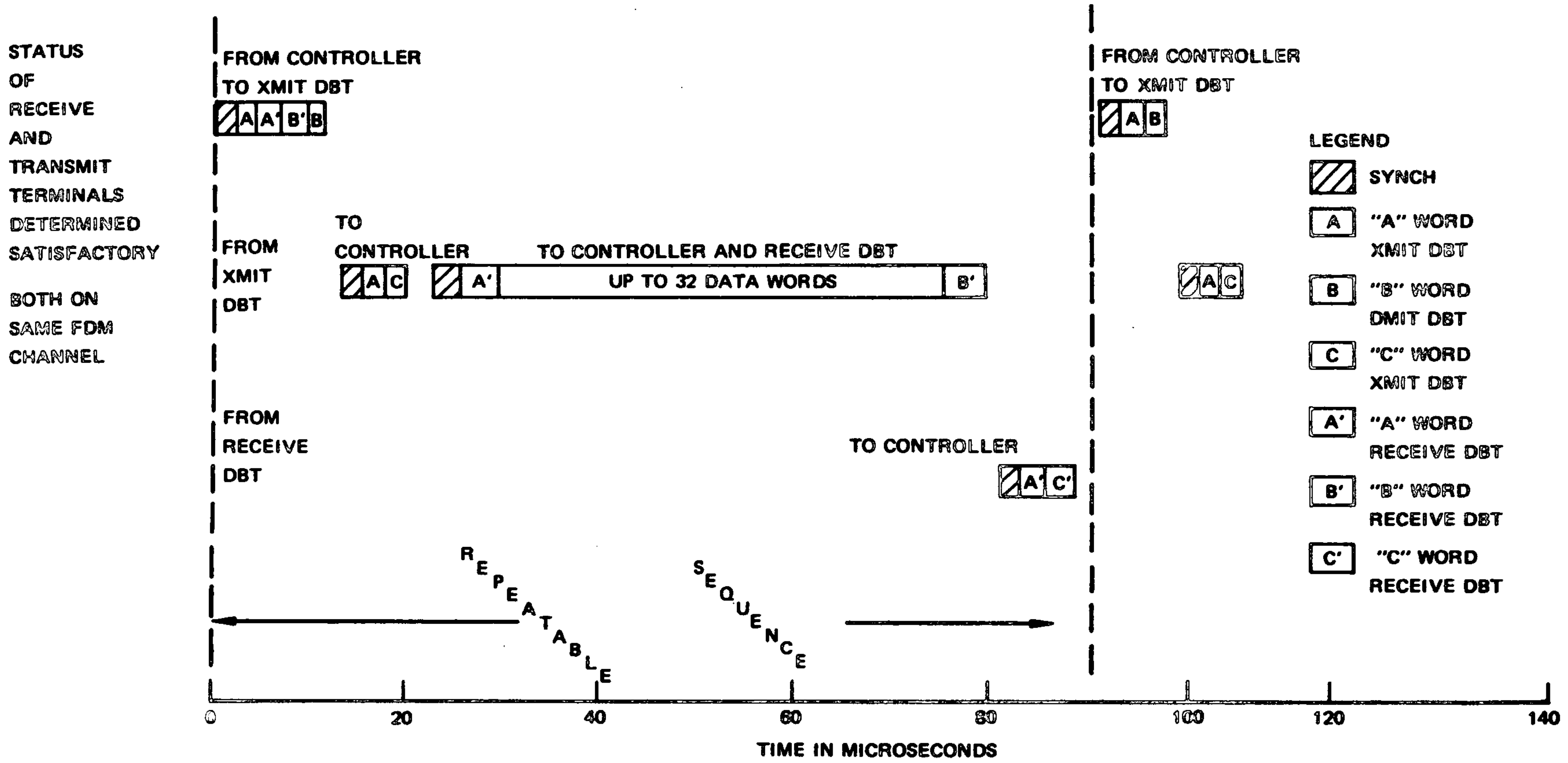


Figure B-6. Terminal–to–Terminal Transfer (TTT) Timing Sequence

B.3.2.2 Physical Characteristics

The physical characteristics for each data bus element shall not exceed the following:

Element	Weight	Power	Volume
DBT - Digital	TBD	TBD	TBD
DBT - Audio	TBD	TBD	TBD
DBT - Video	TBD	TBD	TBD
Coax Cable	TBD	N/A	N/A
Coax Coupler	TBD	N/A	TBD
Coax Terminator	TBD	N/A	TBD
Shielded Pair Cable	TBD	TBD	TBD
RDAU	TBD	TBD	TBD

B.3.2.3 Reliability

Failure rates (per unit) per million operating hours shall not exceed the following:

Element	Failure Rate
DBT - Digital	TBD
DBT - Audio	TBD
DBT - Video	TBD
Coax Cable	TBD
Coax Coupler	TBD
Coax Terminator	TBD
Shielded Pair Cable	TBD
RDAU	TBD

B.3.2.4 Maintainability

The capability shall exist to isolate, replace, and return the major malfunctioning elements to a fully operational status within 1 hour after malfunction detection.

B.3.2.5 Operational Availability

The capability shall exist to support selected subsystem operations at all times in orbit.

B.3.2.6 Safety

Safety requirements shall be in accordance with the safety requirements of the MSS specification (TBS).

B.3.2.7 Environment

The environmental requirements shall be in accordance with the natural and induced environments specified in the MSS specification (TBS).

B.3.3 Design and Construction Standards

Design and construction standards shall be in accordance with MSS specification (TBS). Unique design and construction requirements will be accommodated on an "add or delete" basis.

B.3.4 Logistics

Logistics requirements shall be in accordance with those of MSS specification (TBS).

B.3.5 Personnel and Training

Personnel and training requirements shall be in accordance with those of MSS specification (TBS).

B.3.6 Interface Requirements

Interfaces between data bus elements and with other MSS elements are indicated as follows.

B.3.6.1 Power

The following power will be supplied to the data bus elements: TBD.

B.3.6.2 Cooling

The following provisions will be made for cooling data bus elements: TBD.

B.3.6.3 Mounting

The following provisions will be made for installation of the data bus elements in the MSS: TBD.

B.3.6.4 IOC-DBT

The IOC computing assembly shall communicate with the data bus in accordance with the word formats and timing defined in B.3.2.1.6.

B.3.6.5 Data Bus to Subsystems or Experiments

The data bus will interface with subsystem or experiment elements through standardized data bus remote data acquisition units or customized subsystems or experiment interface units considered to be supplied with each subsystem or experiment.

B.3.7 Requirements for Data Bus Elements

Performance and design requirements for data bus elements are specified in the subparagraphs below. The input/output controller (IOC) is a computing assembly which is not a part of the data bus. Pertinant IOC specifications are included to illustrate the interrelationship between the IOC and data bus elements.

B.3.7.1 Digital Data Bus Terminal

The digital data bus terminal shall contain the necessary logic, buffering, and control to interconnect the data bus with the following units:

A. Remote data acquisition units (RDAU).

B. Customized subsystem interface units and experiment interface units.

C. Direct connection to subsystem and experiment elements.

The data bus terminal interfaces shall be in accordance with Figure B-7. The DBT logic shall accept 10-MBPS Manchester Type II biphase coded digital data from the modem, decode the address and functional codes, and perform the necessary steps to execute the particular command. The

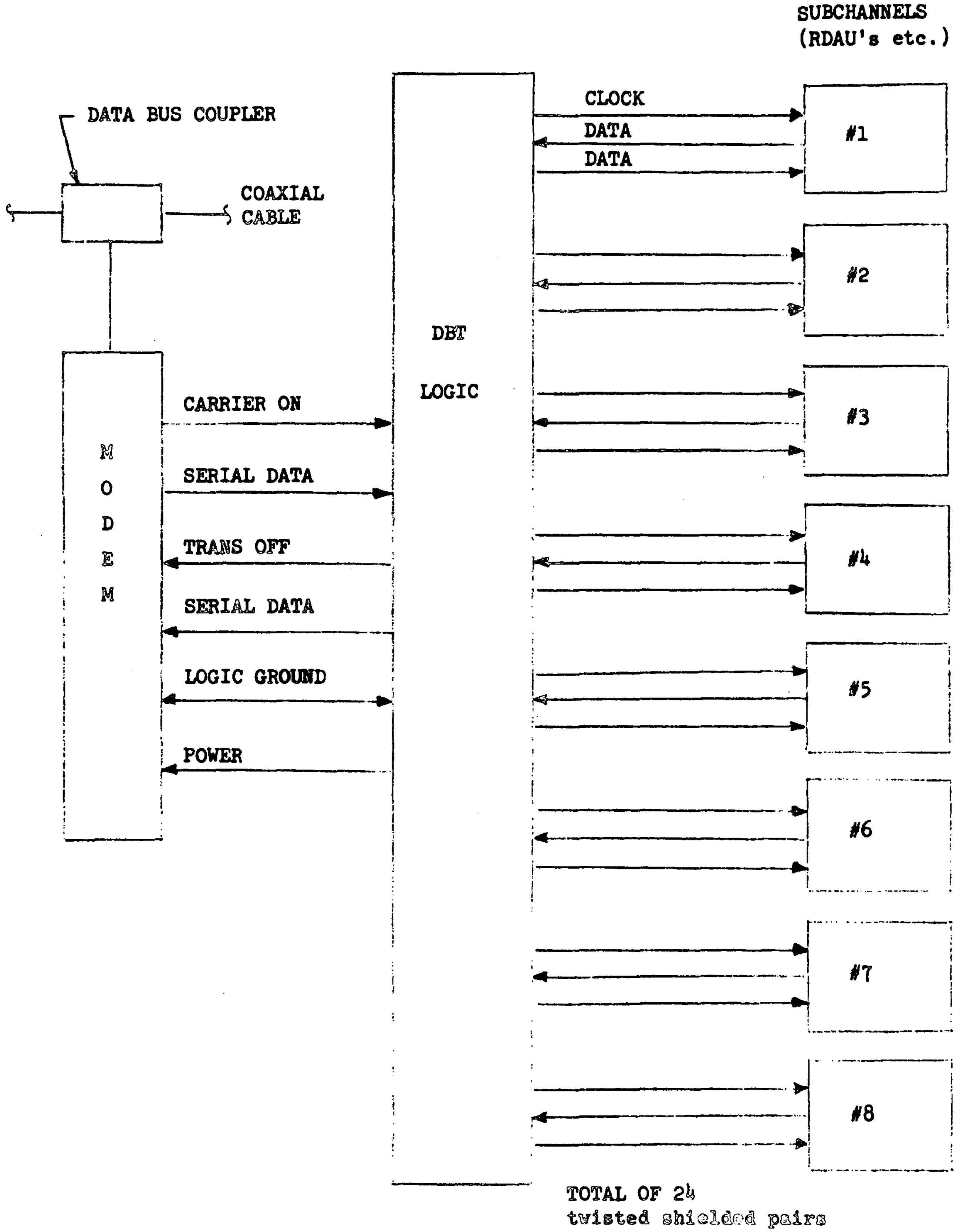


Figure B-7. Data Bus Terminal Interfaces

DBT shall interface with one of 8 I/O channel devices at 1 MBPS with a bipolar NRZ code. Each DBT shall respond only to a uniquely assigned hardware programmable address. Each DBT shall contain up to three pluggable modems, which are specified in Section B.3.7.2.

B.3.7.2 Modems

The digital DBT modems shall interface with the bus controller, transmission line, and data bus terminal logic to provide compatible input/output characteristics. The modem shall accept Manchester Type II biphase coded data at 10 MBPS and modulate this waveform on an rf carrier of 140, 210, or 300 MHz. The transmitter out-of-band characteristics shall be in accordance with Figure B-8. The total transmitted power shall be approximately 16 dbm.

The modulated RF carrier shall be accepted by the receiver portion of the modem. The receive section of a transmitting modem shall be turned off during the transmit cycle to prevent overloading and possible erroneous operation. The 10 MBPS Manchester coded waveform shall be derived from the detector and transmitted to either a data bus terminal or the bus controller. The receiver out-of-band characteristics shall be in accordance with Figure B-9, where the bandwidth is 25 MHz to accommodate the 10 MBPS waveform.

B.3.7.3 Couplers, Cable, and Terminator

The data bus shall be kept in a matched condition for optimum operation by the use of three-port couplers.

Each of these connectors shall have a characteristic impedance of 75 ohms to match the data bus low loss 75-ohm cable characteristics. Terminators shall be used to match the characteristic impedance at the ends of the coaxial cable.

B.3.7.4 Remote Data Acquisition Units

The RDAU shall perform the following operations:

A. Signal conditioning shall be accomplished through preconditioning networks of the analog multiplexer and a programmable gain

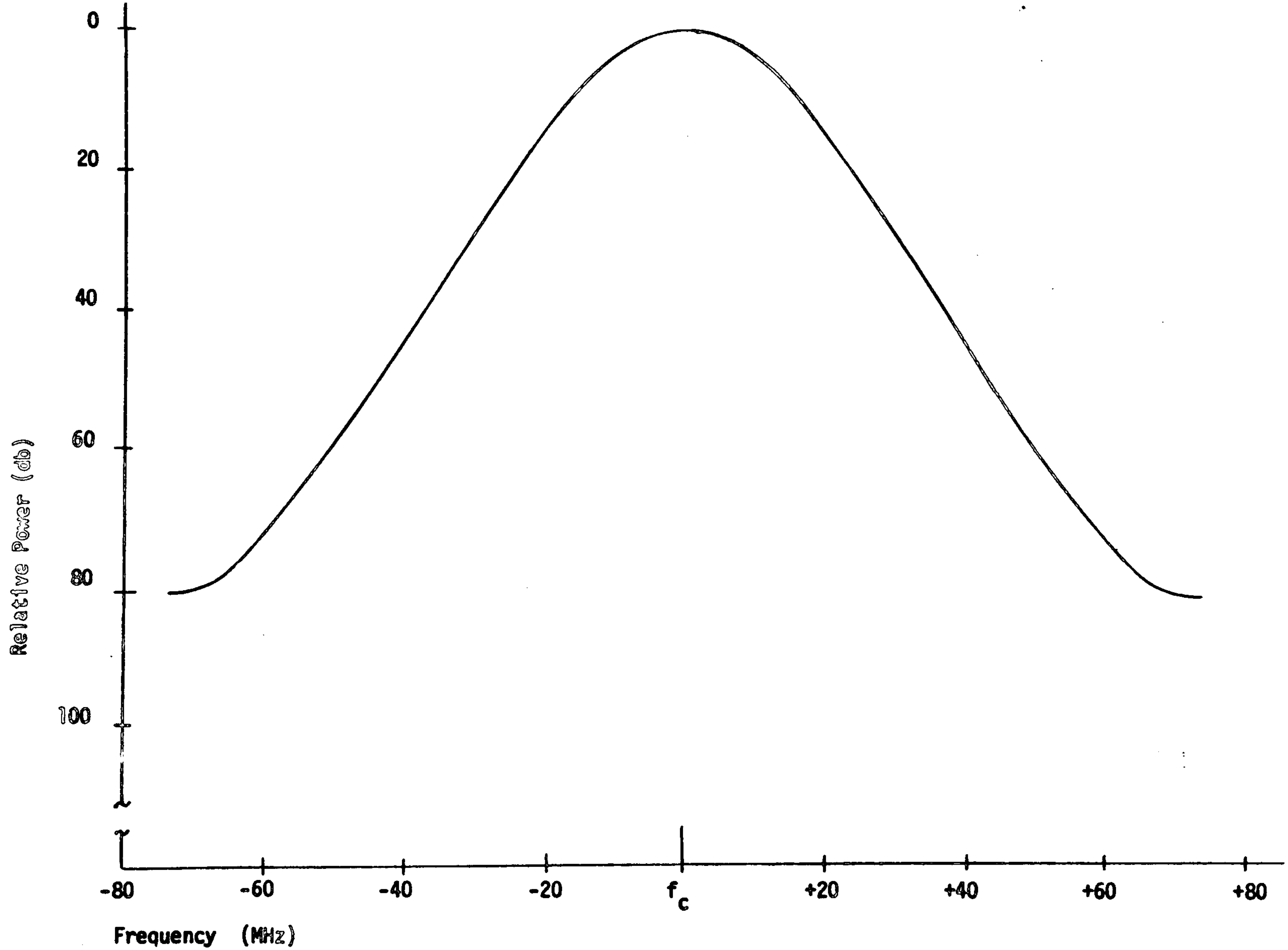


Figure B-8. Modern Transmitted Relative Power Spectrum

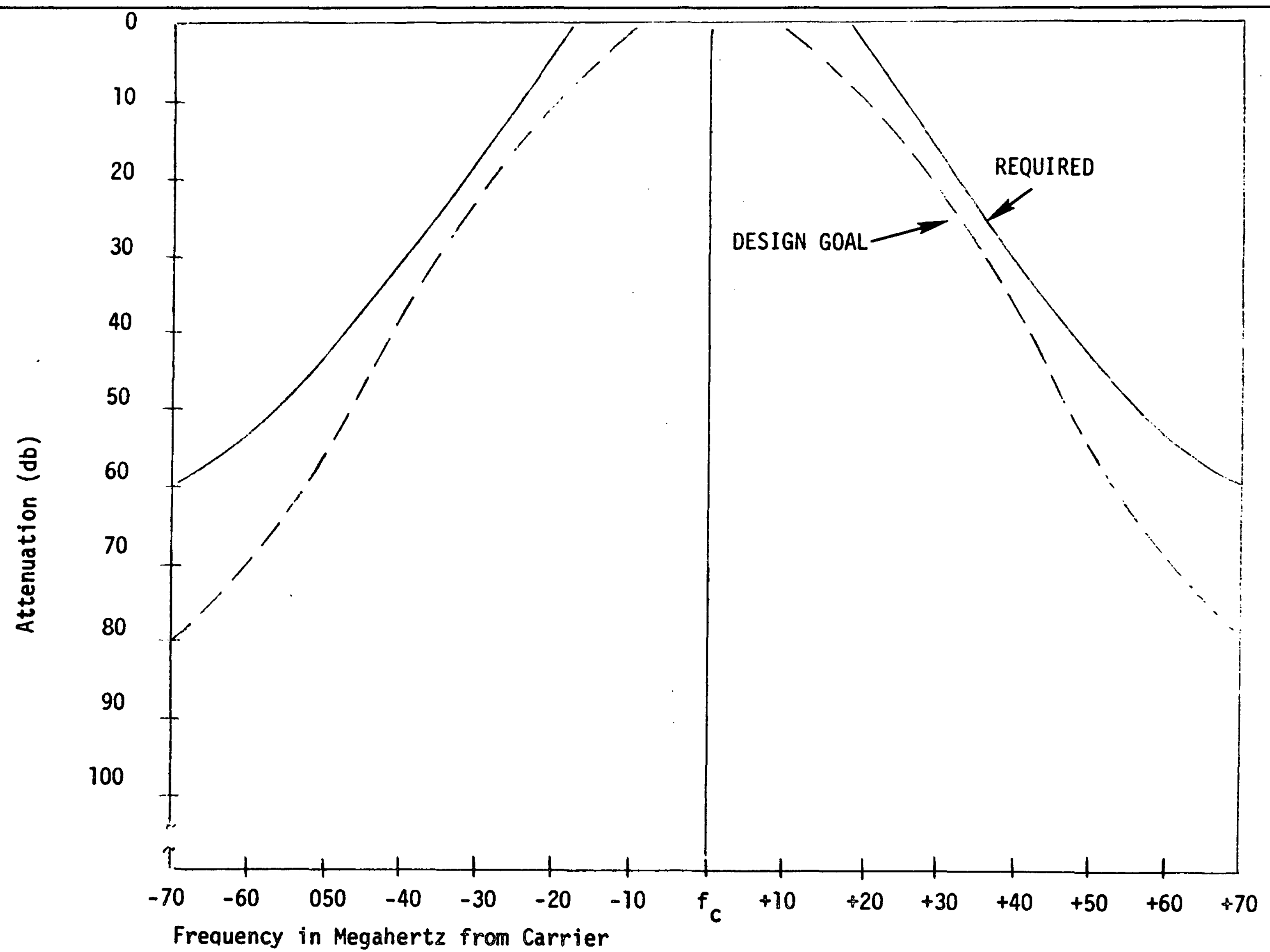


Figure B-9. Minimum Receiver Response

amplifier immediately following multiplexing. The signal conditioning shall provide the required gain/bandwidth characteristics required for a particular application.

B. Both analog and digital multiplexing circuits shall be provided to accommodate up to 16 channels of digital data multiplexed in groups of 8, and up to 30 analog channels. The multiplexers shall handle any combination of analog channels and any combination of sets of eight (8) digital channels.

C. The A/D conversion bit rate shall equal the clock rate in the RDAU. The A/D converter output shall be digitally compared with high and low limits extracted from a self-contained memory. If the measured parameter exceeds either limit, the return data shall be flagged with the out-of-limit channel address as an out-of-tolerance condition.

D. The control logic shall allow for 16 control function outputs to provide on-off control. A separate control signal shall switch to either the on or off state.

B.3.7.5 Input/Output Controller

The input/output controller shall perform the following functions:

A. Control all data bus information flow.
B. Control the acquisition of data for onboard data processing.
C. Control the transmission of data from the digital computer and main memory to other subsystem elements.

These functions are performed by two units:

A. Computer interface unit (CIU).
B. Subsystem interface unit/computer (SIU/C).

All IOC functions shall be under the supervision of the central processor unit (CPU). The IOC shall consist of a computer interface unit and a subsystem interface unit/computer.

B.3.7.5.1 Computer Interface Unit

The computer interface unit (CIU) shall:

A. Receive, decode, and control the execution of input/output commands initiated by the CPU.

B. Fetch detailed input/output control sequences from main memory and execute these control sequences.

C. Fetch data from main memory for transmission to the data bus via the SIU/C.

D. Serialize commands and data to be transmitted.

E. Deserialize information received from the data bus.

F. Provide for transmitting data and commands to as many as three data bus channels simultaneously.

G. Provide for receiving data from as many as three data bus channels simultaneously.

NOTE: For Items F and G the total number of data bus channels is three. Any one channel may transmit or receive on the same frequency, but not simultaneously.

H. Provide for controlling and performing bidirectional communications with auxiliary memory units.

I. Provide buffer storage for data and commands being communicated to and from the data bus.

J. Control the storage of information received from the data bus into main memory.

K. Provide timing and internal synchronization.

L. Signal the CPU upon termination or completion of data communications.

M. Generate parity bits and test for parity for information stored and fetched from memory.

N. Provide for testing of IOC operational status under CPU control.

O. Monitor status of data integrity and signal the CPU upon failure of integrity tests.

B.3.7.5.2 Subsystem Interface Unit/Computer (Modem)

The SIU/C shall consist of up to three sets of transmitter and receivers and associated modulation, demodulation, circuitry, filtering, and signal conditioning called "modems." Each modem operates on a carrier frequency separate from other modems and will use the same carrier frequency for both transmitting and receiving. Each modem will be capable of transmitting and receiving digital information at rates as high as 10 MBPS.

The functional requirements of the modulator-transmitter portion of each modem shall be:

A. Apply remodulation filtering and signal conditioning to input signals from the computer interface unit.

B. Modulate the modem carrier.

C. Filter the modulated output to confine the signal to its allocated bandwidth.

The functional requirements of the receiver-demodulator portion of each modem shall be:

A. Filter the modulated carrier input from the data bus according to carrier frequency and bandwidth requirements.

B. Demodulate the modulated carrier input.

C. Condition the digital output signals to specified voltage levels.

B.3.7.6 Audio Data Bus Terminal: TBD.

B.3.7.7 Video Data Bus Terminal: TBD.

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Appendix C

DATA BUS BREADBOARD SPECIFICATION
IMS-DB-001A

C.1 SCOPE

This specification establishes the requirements for the design and performance of the information management subsystem digital data bus breadboard.

C.2 DATA BUS UNITS

The data bus shall consist of the following units.

C.2.1 Bus Interface Unit

A bus interface unit (BIU) which interfaces with a processor I/O channel and provides control of the data bus.

C.2.2 Transmission Line

A transmission line consisting of:

A. Coaxial cable(s).
B. Terminators.
C. Couplers.

C.2.3 Modems

Modems which interface with the transmission line, bus interface unit, and terminals to provide compatible input and output characteristics.

C.2.4 Terminals

Terminals contain the necessary logic, buffering, and control to interconnect the data bus transmission line, through modems, to the following units:

A. Remote data acquisition units (RDAU).
B. General and special purpose computer I/O.
C. Digital tape controllers.
D. Manual keyboards.
E. Special subsystem and experiment interface units.

C. 3 DATA TRANSFER REQUIREMENTS

C. 3. 1 Performance Requirements

C. 3. 1. 1 System Functional Requirements

C. 3. 1. 1. 1 System Performance Requirements

The information management subsystem data bus breadboard shall be capable of distributing digital signals throughout the information management subsystem.

C. 3. 1. 1. 1. 1 Multiplex Type

The data bus shall use frequency division multiplexing (FDM). All digital signals are assigned to time division/frequency division multiplexed (TDM/FDM) channels. The digital channels shall use double-sideband amplitude modulation (AM) for modulating subcarriers.

C. 3. 1. 1. 1. 2 Data Bus Routing

The data bus shall incorporate a communication network consisting of coaxial cable extending a maximum distance of 500 feet.

C. 3. 1. 1. 1. 3 Channels

On the Space Station, the data bus shall be capable of providing the following channels: addressing capability for up to 8 digital channels capable of distributing biphase signals at rates up to 10 MBPS with bit errors less than one in 10^7. Three channels will be located in the frequency range of 140 to 300 MHz, with Double Sideband Amplitude Modulation (DSAM) techniques and a detected signal-to-noise ratio of at least 22 db. Channels 1, 2, and 3 shall have center frequencies of 140, 210, and 300 MHz, respectively.

C. 3. 1. 1. 1. 4 Grounding

The primary power ground or return shall be isolated from the coaxial cable shield. The internal circuit ground shall be isolated from chassis ground, and the resistance between the two shall be a minimum of 2 megohms at 25 vdc.

C. 3. 1. 1. 1. 5 Failure Protection

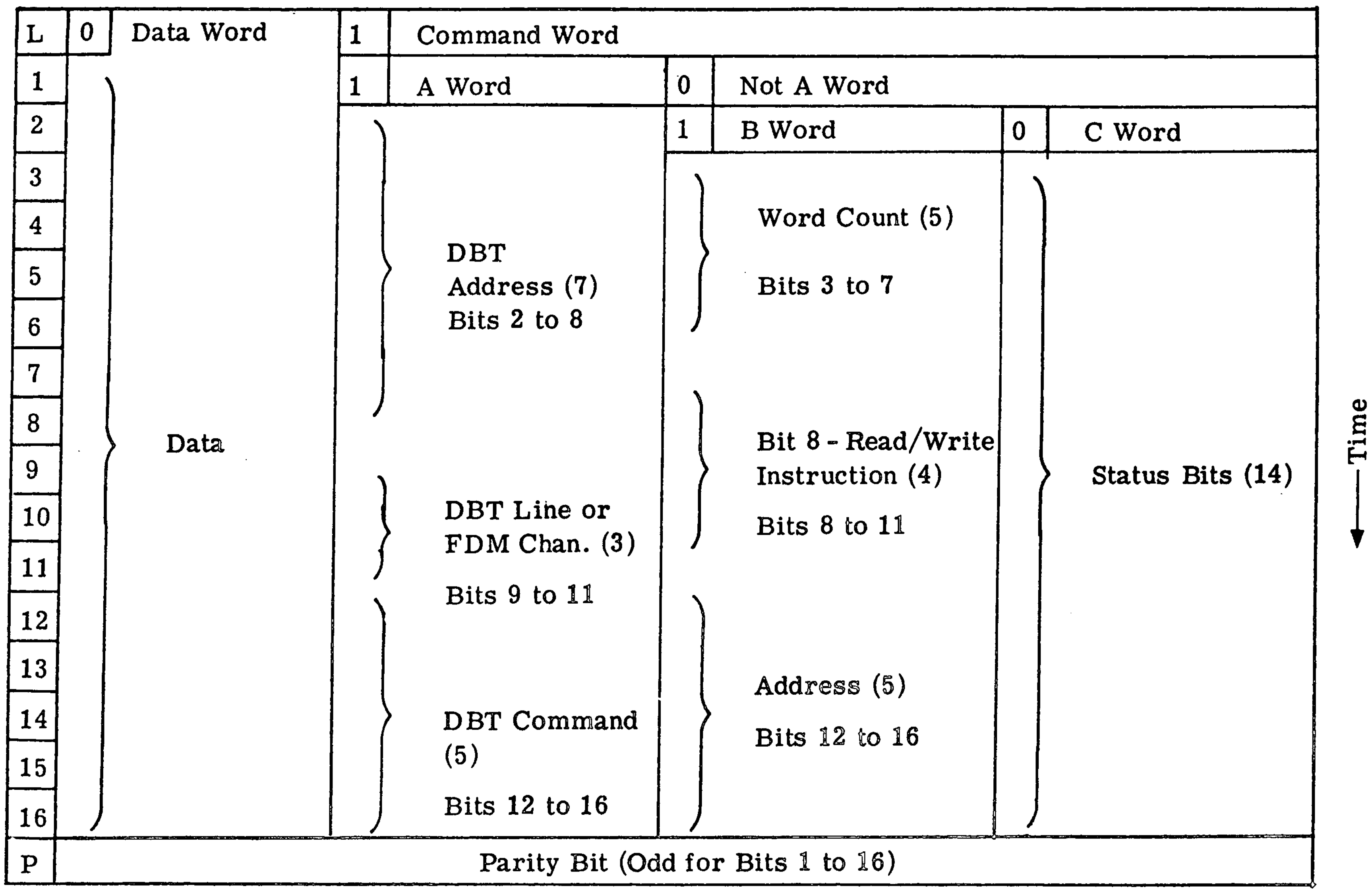
In the event of a unit failure, the designs shall present a fail-safe mode; e. g., modems will be designed to fail open and the transmission lines will be designed such that a normal failure will be in the shorted mode. A normal failure in one channel shall not affect other channel operation. A redundant data bus shall be provided to allow manual switchover, remotely controlled switchover, and automatic switchover to allow normal equipment operation while maintenance is performed on the failed unit.

C. 3. 1. 2 System Operation

All communications or messages in data bus digital channels will either be "commands" generated by the BIU or "responses" generated by one of the data bus terminals (DBT). These messages will be transmitted in an ordered sequence and consist of a combination of 18-bit words.

C. 3. 1. 2. 1 Message Formats

Figure C-1 shows the word formats for information transfer over the data bus. Four types of 18-bit words are identified as "A," "B," "C," or "D" words. An "A" word contains the DBT address and command; a "B" word contains a word count, the device instruction, and the device channel address; a "C" word contains status; and a "D" word contains data. The address portion of the "B" word shall be 00000 if not indicating an address. Command messages occur in the form of an "A" word, following by data if any, and ending with a "B" word. A normal response to a command consists of the echoed "A" word, following by up to 32 data ("D") words, and ending with a "C" word. Each bus transmission starts with a synchronization burst (C. 3. 1. 6. 1. 2) following by an "A" word, data if any, and ends with either a "B" or "C" word. In a device-to-device transfer, an additional "A" and "B" word (designated hereafter as A' and B') are transmitted from the BIU to the DBT as two data words; i. e., having identical formats as an "A" and "B" word, but containing a lead zero rather than a lead one. This data provides the address of the second device and contains any necessary control information. The DBT then reinserts the lead ones and uses these data words as control words for device-to-device transmissions.



L = Lead Bit
P = Parity Bit

Figure C-1. Data Bus Word Formats

C. 3. 1. 2. 2 System Timing
Information transfers between data bus connected devices occur in the formats specified in C. 3. 1. 2. 1. This paragraph describes the timing of each sequence.

Transfers between the BIU and DBT are illustrated in Figures C-2 and C-3. Figure C-2 shows the normal sequence for transfer of data from the DBT to the BIU (identified as a read mode). In a typical read sequence, the BIU transmits synch, an "A" word, and a "B" word to the DBT. This requires something less than 6 microseconds. In response, the DBT generates a synch burst, an echo "A" word, up to 32 16-data-bit plus 2 control-bit data words, and ends with a "C" word containing terminal status information. This requires approximately 63 microseconds. The total response time (from time of command initiation to receipt of message) is approximately 73 microseconds with circuit and propagation delays accounting for approximately 4 microseconds. In the event special data is required from an I/O device such as a remote data acquisition unit (RDAU), a special request sequence must be serviced whereby a large time delay of 738 microseconds is allowed for data transfer from an I/O device to the DBT at 1 MBPS. The BIU issues a command consisting of synch, an "A" word, and a "B" word. This requires approximately 6 microseconds. The DBT responds with a synch, an echoed "A" word, and a "C" word. This also requires approximately 6 microseconds. After a delay of 8 microseconds, the DBT transmits the "B" word to the I/O device (hereafter assumed to be an RDAU). This transfer requires approximately 19 microseconds. The RDAU responds within 4 to 14 microseconds with the data transfer taking up to 576 microseconds for a total elapsed time of approximately 733 microseconds allowing for circuit and propagation delays. The typical read sequence is then initiated to bring data to the BIU. Total elapsed time will be less than 810 microseconds. The data bus channel is only occupied for 85 microseconds and other functions can be performed during the channel free time.

Figure C-3 illustrates the typical write mode. The BIU transmits a synch, an "A" word, up to 32 18-bit data words, and a "B" word, requiring 63 microseconds. The DBT responds with a synch, an echoed "A" word, and a "C" word. After a delay of 8 microseconds, a "B" word is

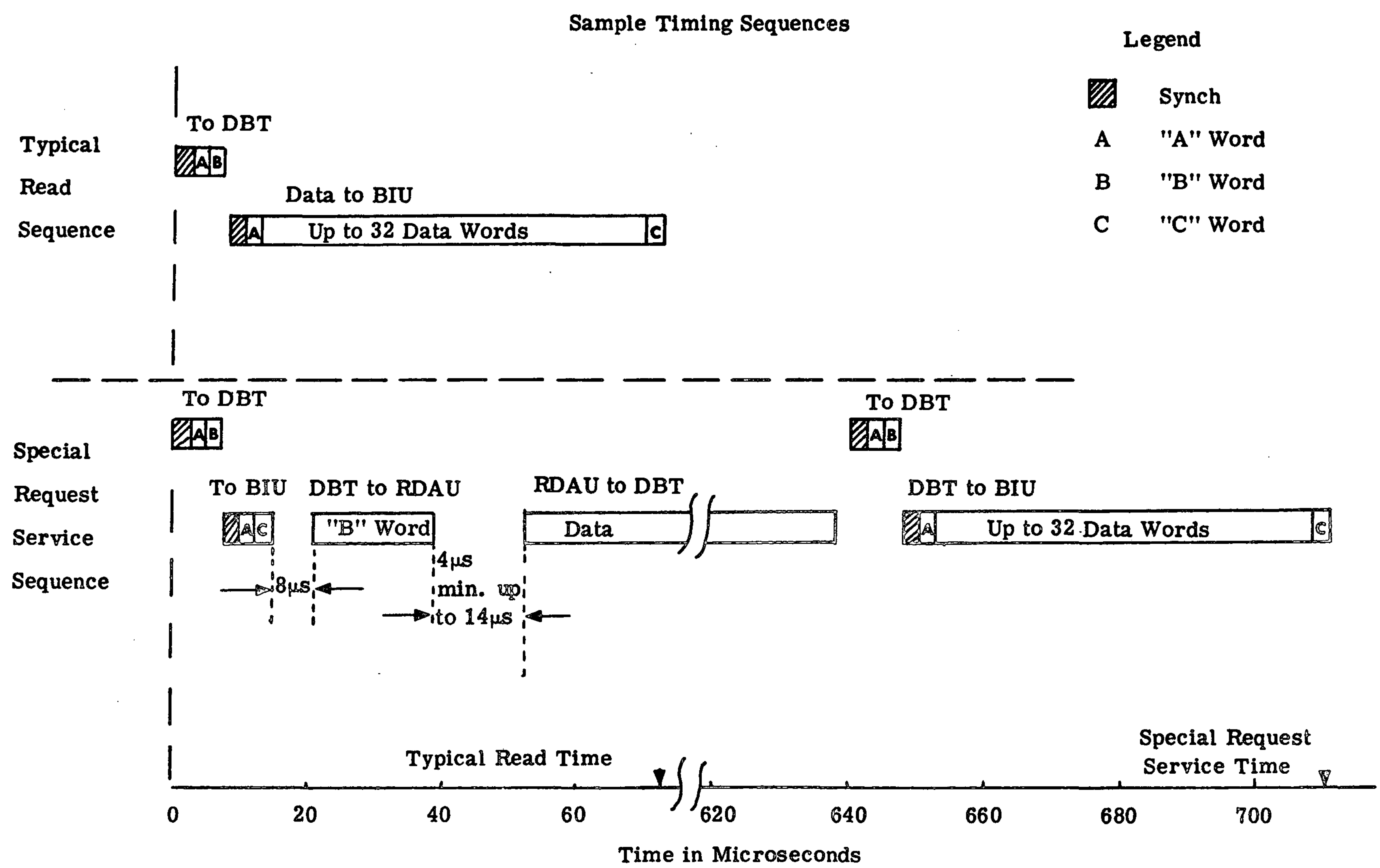


Figure C-2. Read Sequence Timing

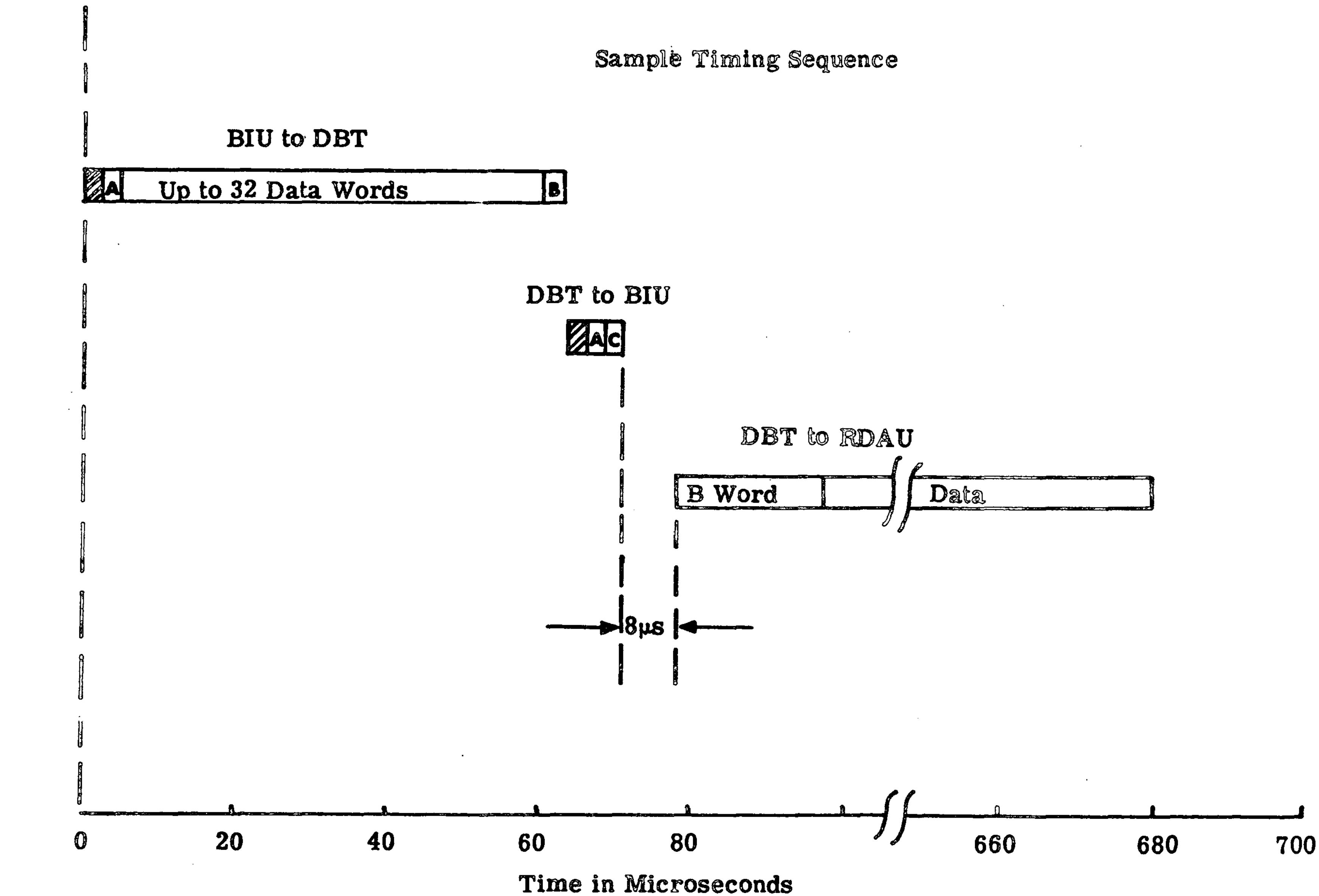


Figure C-3. Write Sequence Timing

transmitted to the RDAU followed by up to 32 data words. Total elapsed time will be less than 680 microseconds. The data bus channel is only occupied for approximately 12 to 73 microseconds, however, and can be utilized to perform other functions.

The sequence for terminal-to-terminal information transfer is shown in Figure C-4. In the event that both terminals are not on the same channel, a preliminary command must be sent to switch one of the terminals (identified by the address of the "A" word) to the other's frequency channel. This sequence is not shown in the figure. The BIU transmits a synch, an "A" word, and A' data word, a B' data word, and a "B" word. The DBT responds with a synch, an "A" word, and a "C" word. After a nominal delay time (approximately 1 microsecond), the DBT transmits another synch, the A' word, up to 32 18-bit data words, and the B' word. The DBT identified by the address field in the A' word receives the data and responds with a synch, an echoed "A" (A') word, and a "C" word. This sequence is repeatable with A' and B' words issued with each terminal-to-terminal transfer sequence. The total sequence will require less than 84 microseconds but occupies the data bus channel for the full amount of time. Therefore, the data bus channel is occupied for the total length of time required for terminal-to-terminal transfer. The reset command is issued to the DBT identified by the "A" word to reset the FDM channel, if necessary, and to reset the registers containing the A' and B' words.

C. 3. 1. 3 System Interface Requirements

The data bus shall be designed such that a constant impedance is reflected to the transmission line, regardless of the number of active devices on the line. Each digital channel shall be capable of terminating a minimum of 64 stations.

C. 3. 1. 3. 1 Terminations and Connections

Each terminal connection shall exhibit the transmission line characteristic impedance and shall have the specific characteristics defined in C. 3. 1. 5.

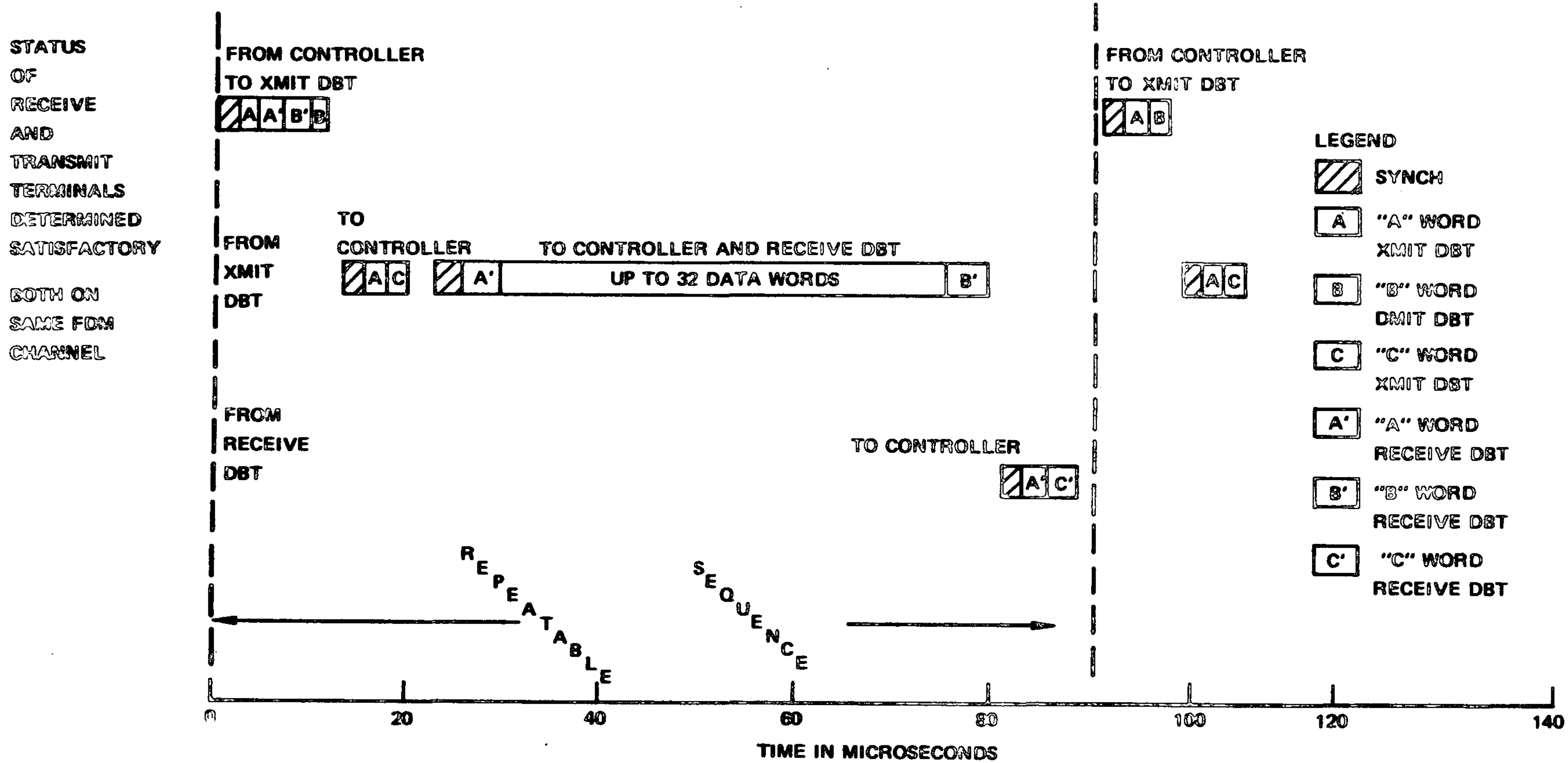


Figure C-4. Terminal-to-Terminal Transfer (TTT) Timing Sequence

Each attached module shall be connected to the data bus by a branch coupler (a three-port coaxial cable coupler specified in C. 3. 1. 5. 1). Each of these connecting points shall be terminated with a dummy termination exhibiting the transmission line characteristic impedance when an attached module is not present. The data bus connecting diagram is shown in Figure C-5.

C. 3. 1. 4 Modem Functional Requirements

C. 3. 1. 4. 1 Modem Performance Requirements

C. 3. 1. 4. 1. 1 Receiver

A. RF Bandwidth—25 ±0. 5 MHz.

B. Dynamic Range—40 db minimum.

C. Receiver Settling Time—The receiver shall be capable of responding to an input signal within 0. 8 microseconds maximum after the presence of the carrier.

D. Detection—Noncoherent detection.

E. Sensitivity—Minus 92 dbm minimum with the specified bandwidth and noise figure at 20°C ambient temperature.

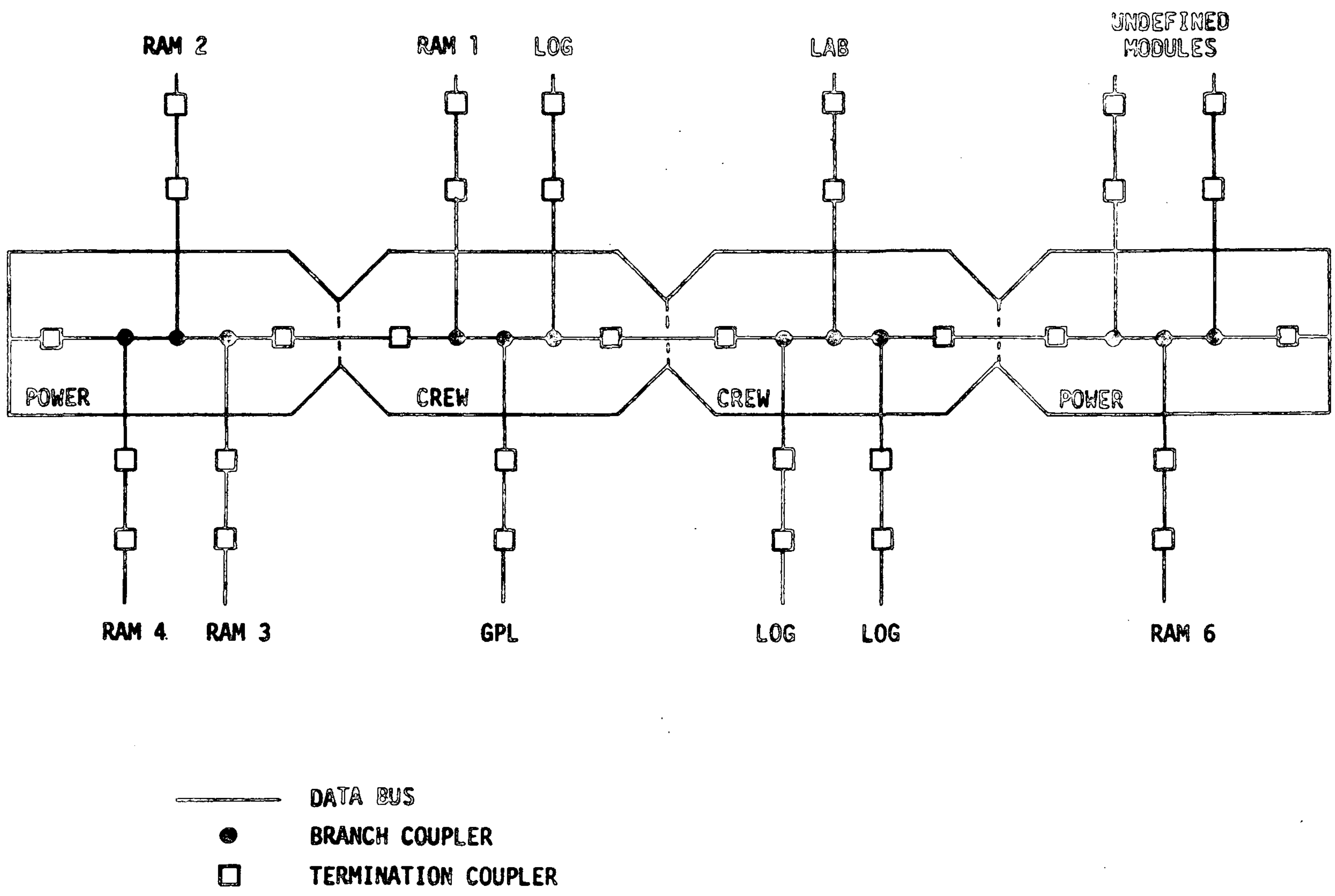
F. Noise Figure—8 db maximum.

G. Out-of-Band Rejection—The receiver shall have out-of-band rejection characteristics with attenuation relative to that at the carrier center frequency (f_c) as follows:

   1. $f_c \pm 30 \geq 15$ db
   2. $f_c \pm 50 \geq 45$ db
   3. $f_c \pm 60 \geq 55$ db
   4. $f_c \pm 75 \geq 60$ db

H. Maximum Power Input—The receiver shall be capable of withstanding a maximum input power of 16 dbm.

I. Phase/Delay Distortion Characteristics—The phase/delay characteristics from f_c (carrier frequency) to $f_c \pm 30$ or greater shall approach that of an eight-section Gaussian bandpass filter with cutoffs at f_c + 15 MHz and f_c - 15 MHz. Delay at the $f_c \pm 30$ MHz points shall not exceed the delay at $f_c \pm 10$ MHz by more than 30 monoseconds.



NOTE: Same connection concept for both Analog and Digital Buses.

Figure C-5. Data Buses Connection Diagram

C. 3. 1. 4. 1. 2 Transmitter

A. Unmodulated Carrier Power Output—20 dbm ±1 db.

B. Frequency Stability—The modem transmitters shall exhibit no more than 100 KHz drift from the specified center frequency at temperatures from 0° to 50°C.

C. Attenuation Characteristics—The transmitter output shall have the frequency attenuation characteristics defined in Figure C-6.

D. Inband Amplitude-Phase Characteristics.

C. 3. 1. 4. 2 Modem Interface Characteristics

The modem interfaces are identified in Figure C-7 and perform the following functions.

A. Serial Data Input—Connects digital data from the DBT's or BIU's to the modem.

B. Serial Data Output—Connects digital data from the modem to data bus terminals (DBT) and/or bus interface units (BIU).

C. Logic Signal Ground—Provides signal ground connection.

D. Carrier On—Provides a logic one level coincident with the presence of the in-channel carrier.

E. Transmitter Inhibit Command—Provides a logic one level to inhibit transmitter operation. The inhibit is released coincident with the presence of a modulation input on the serial data input line.

F. Provides five lines for the input of +12 volts, +5 volts, power ground, -12 volts, and +28 volts.

G. RF Input/Output—Provides the connection to the data bus for input and output of TDM/FDM data. For the breadboard, the carrier frequency will be 140 MHz.

C. 3. 1. 4. 2. 1 Digital Interface

The model shall accept digital inputs on the serial data input line at rates not to exceed 10 MBPS. The modem will output digital data on the serial data output line at rates not to exceed 10 MBPS. Inputs and outputs shall be bilevel and compatible with TTL circuitry. This specification is outlined in Table C-1. The modem shall accept a Manchester Type II format with a 10-MHz maximum information bandwidth and voltage levels shown in Figure C-8.

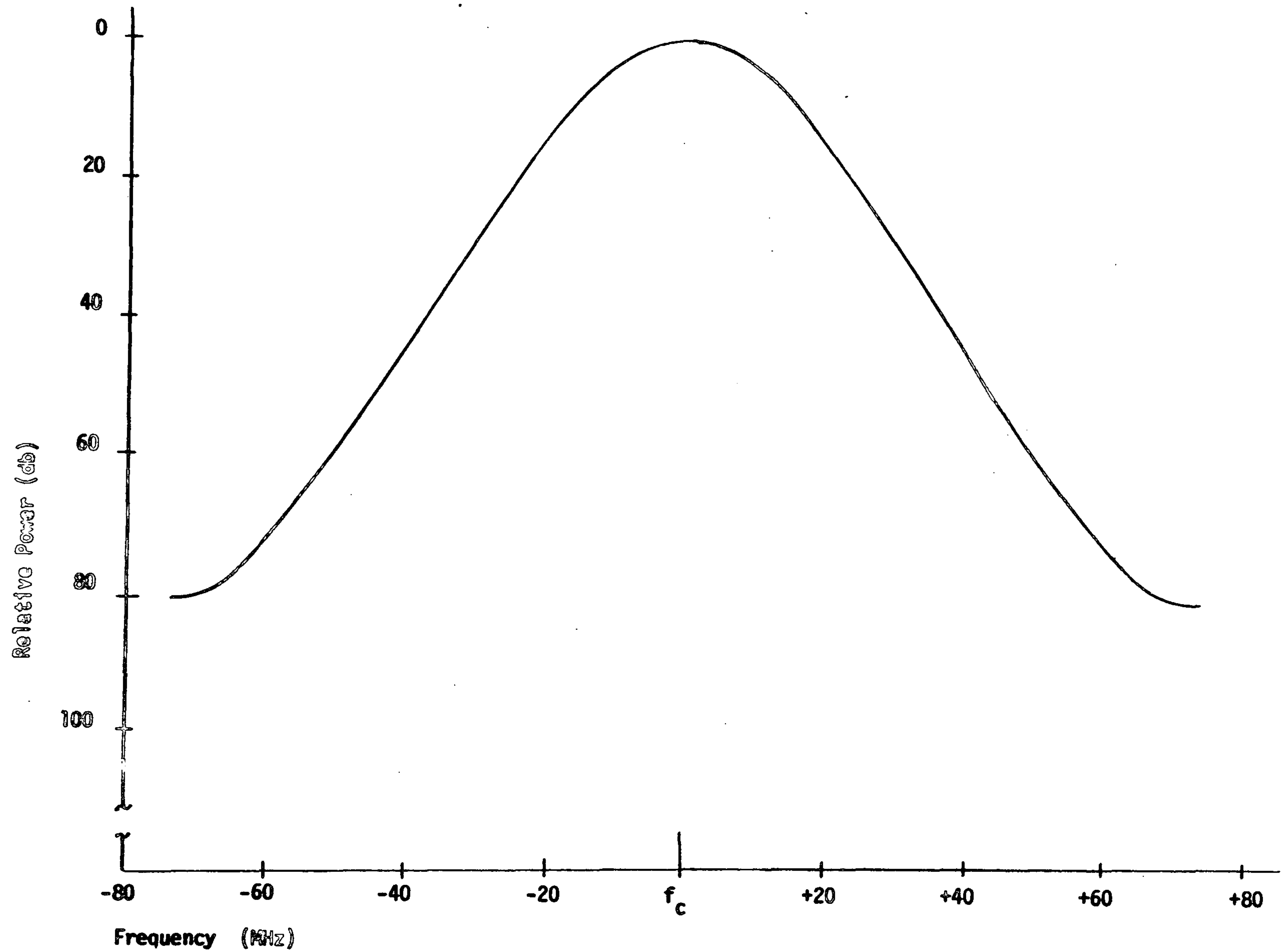


Figure C-6. Modem Power Spectrum

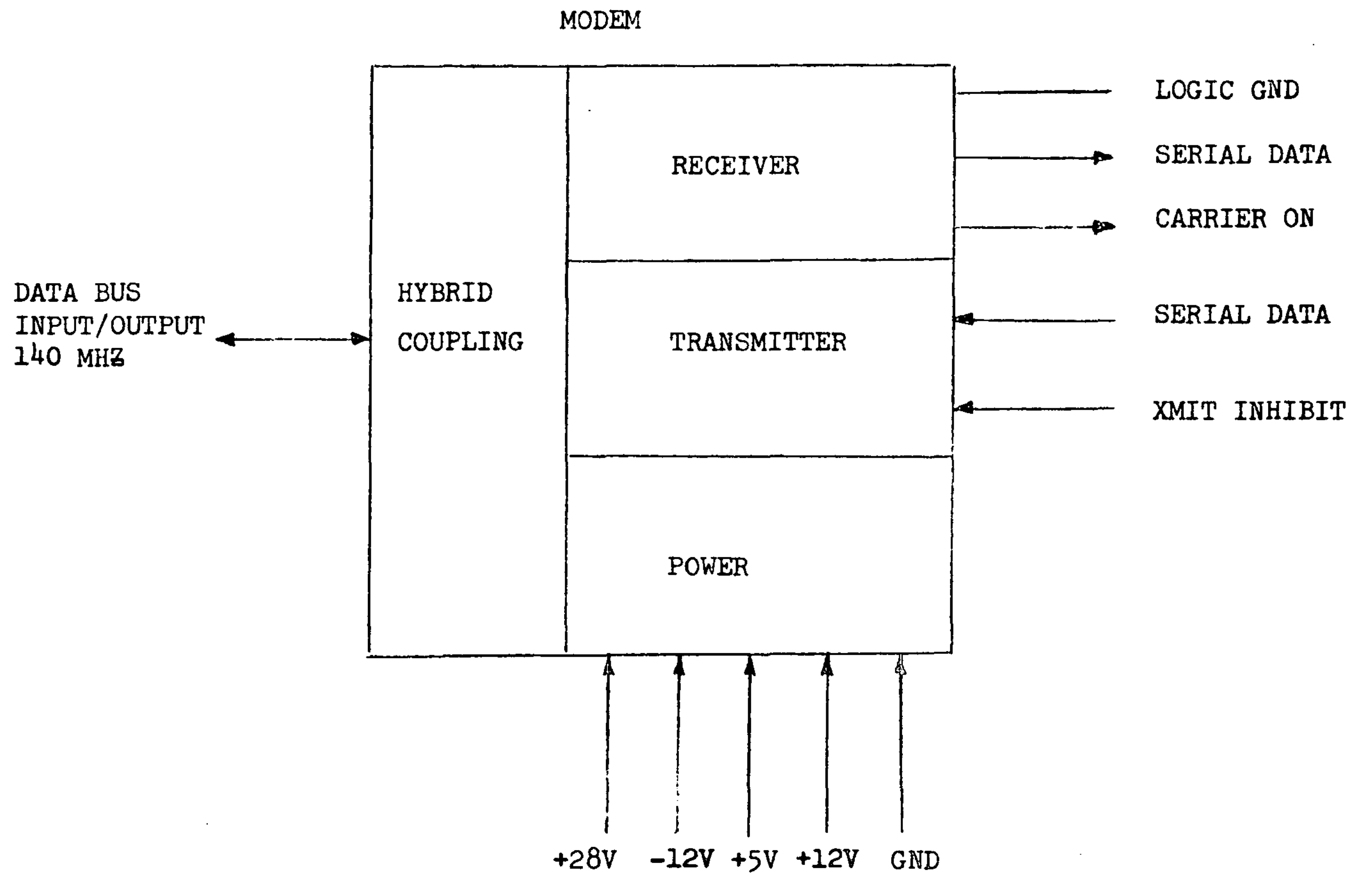


Figure C-7. Modem Interfaces

Table C-1
TTL INTERFACE SPECIFICATION

		Requirement
TTL Output:	Logic one	Greater than 2.4 volts with 0.5 ma load.
	Logic zero	Less than 0.4 volts when sinking 5 ma current.
TTL Input:	Logic one (of plus 2.4 volts)	Input current less than 120 µamps into a positive supply.
	Logic zero (of 0.4 volts)	Input current less than 1.6 ma into a positive supply.

C.3.1.4.2.1.1 Serial Data Input

The serial data input line circuits are TTL compatible and require an input current less than 120 µamps from a positive supply for a logic one of plus 2.4 volts. A logic zero of 0.4 volts or less requires less than 1.6 ma sinked to a positive supply. The rise and fall times, measured between the 10- and 90-percent amplitude points, shall be less than TBD.

C.3.1.4.2.1.2 Serial Data Output

The serial data output line will provide a logic-one greater than 2.4 volts at 0.5 ma load current to ground or 120 microamps to a positive supply. A logic zero will be less than 0.4 volts with a 5 ma or less load current. The rise and fall times, measured between the 10- and 90-percent amplitude points, shall be less than TBD.

C.3.1.4.2.1.3 Carrier On

The carrier on line shall exhibit the same characteristics as those specified in C.3.1.4.2.1.2 and shall assume a positive one level in coincidence with detection of the carrier signal.

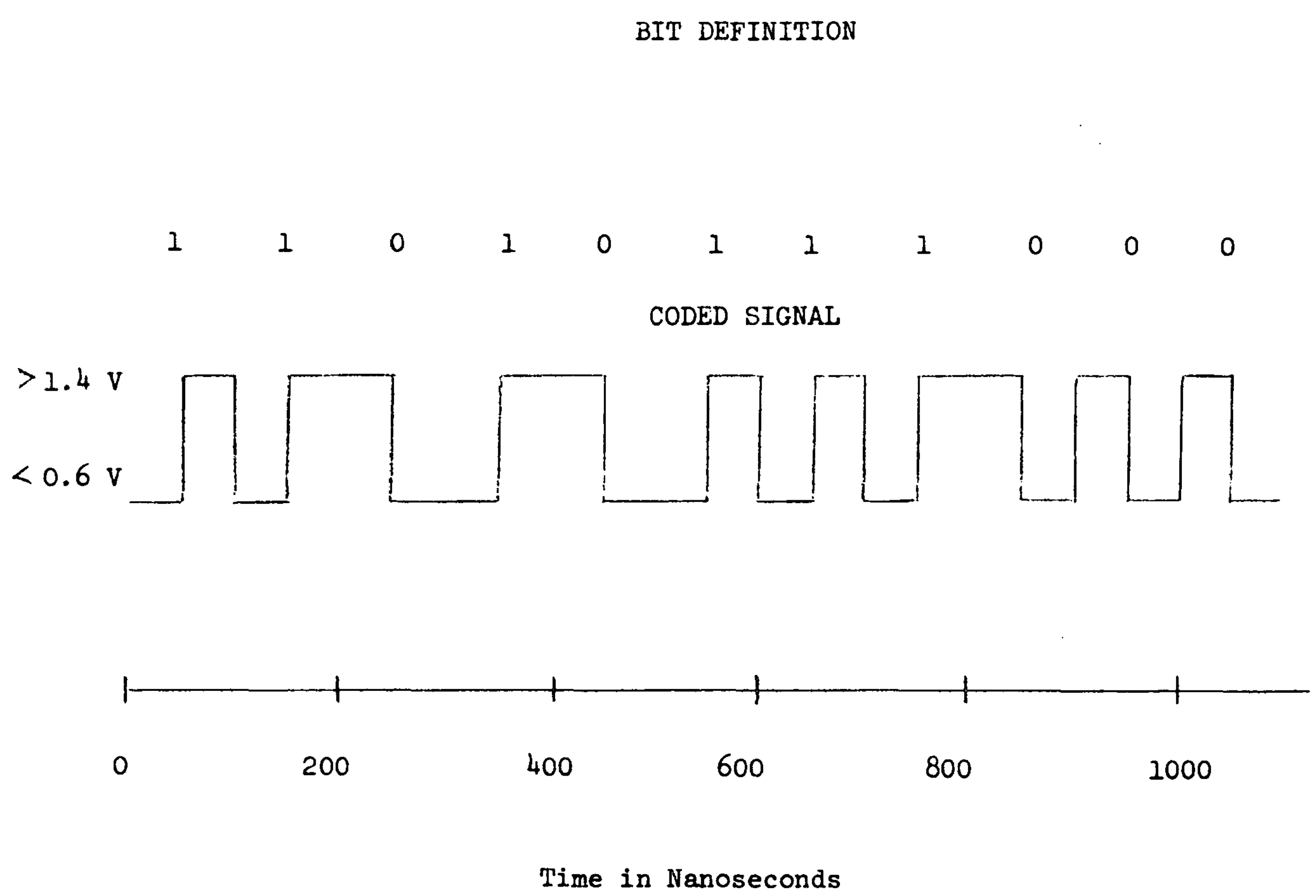


Figure C-8. Manchester Data Format

C. 3. 1. 4. 2. 1. 4 Transmitter Inhibit Command

The transmitter inhibit command line shall exhibit the same characteristics as those specified in C. 3. 1. 4. 2. 1. 1. The signal must be in a logic-zero state before transmission is permitted by the modem.

C. 3. 1. 4. 2. 1. 5 Transmitter Power

The transmitter power line shall be less than TBD volts when the modem is in the receive mode. When in the transmit mode, the transmitter power line shall be greater than 28 volts at less than 700 ma.

C. 3. 1. 4. 2. 1. 6 Power Input

The power input lines shall consist of five lines, +12 volts at TBD ma, -12 volts at TBD ma, +5 volts at TBD ma, +28 volts at 650 ma, and a power spread which shall not rise above TBD volts in relation to logic ground.

C. 3. 1. 4. 2. 1. 7 RF Input/Output

The rf input/output line of the modem is a 75 ohm ±10 percent coaxial cable. The characteristics of this line are defined in C. 3. 1. 4. 2. 2 and C. 3. 1. 4. 2. 4.

C. 3. 1. 4. 2. 2 Rf Interface

The modem shall couple data to and from the data bus transmission line on the data bus input/output line through a combination of a hybrid tee or rf switch and a three-port coaxial cable coupler as in Figure C-9. The carrier frequency shall be at 140 MHz. The connection to the coupler shall be a BNC type connector.

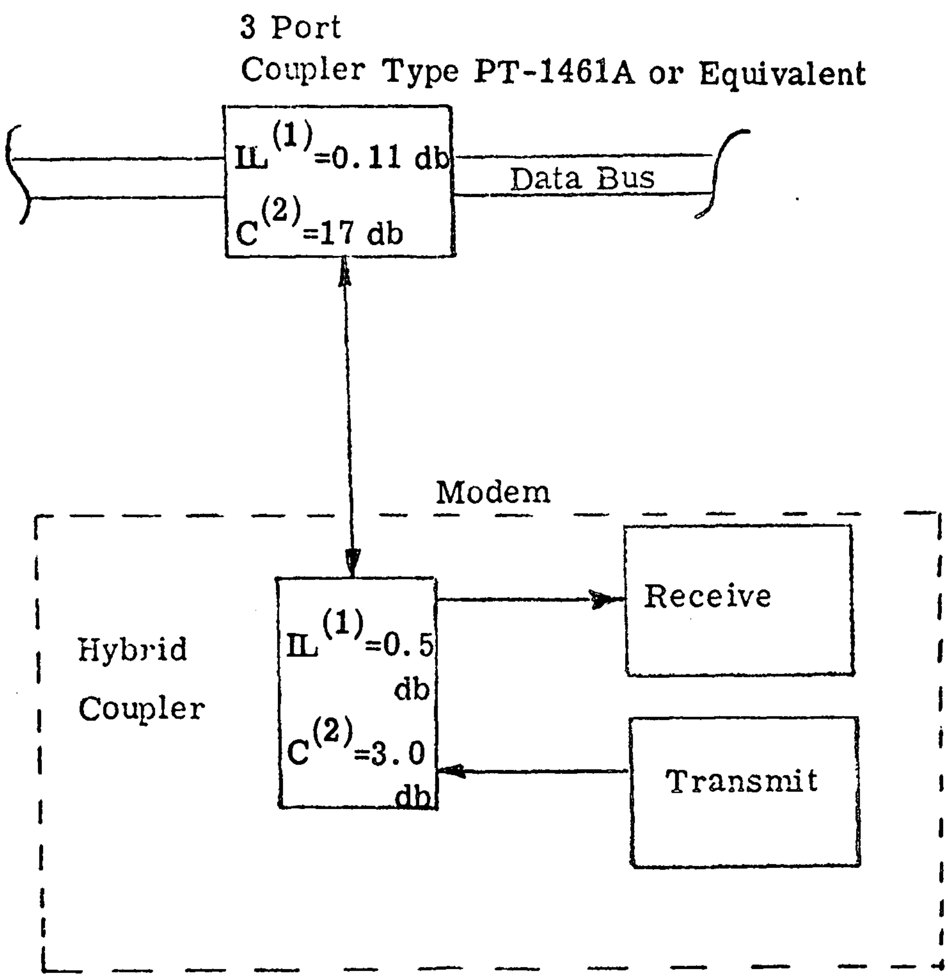
C. 3. 1. 4. 2. 3 Rf Isolation

The modem shall be isolated from the data bus transmission line by the coupling device. The amount of isolation shall be between 10 and 20 db.

C. 3. 1. 4. 2. 4 Rf Input/Output Impedance

The nominal 70-ohm input and output impedances of the modem, interfacing with the transmission line, shall be matched to the coupling device and shall not create more than a 1 to 1. 3 VSWR at the transmission line.

DIGITAL CHANNEL TERMINATION



$IL^{(1)}$ = Insertion Loss At 140 MHz

$C^{(2)}$ = Coupling At 140 MHz

Modem to Data Bus Coupling

Figure C-9. Modem to Data Bus Coupling

C. 3. 1. 4. 2. 5 Modem Connector Assignment

The connector assignment for the modem shall be as shown in Table C-2. Pin functions shall be as shown in Table C-3.

C. 3. 1. 5 Coupler/Cable Functional Requirements

C. 3. 1. 5. 1 Coupler Performance Requirements

A. VSWR—The coupler shall exhibit a VSWR no more than 1.2 to 1 when properly terminated.

B. Coupling Factor—The coupling device shall provide a coupling isolation of 10 db minimum to 20 db maximum.

C. Insertion Loss—The insertion loss associated with each three-port coupler shall be no more than 0.2 db.

D. Impedance—The impedance of the three port coupler shall be 75 ohms ±10 percent at the data bus coaxial cable terminations.

Table C-2

MODEM CONNECTOR ASSIGNMENT

Designation	Name	Part Number
J10	Power and logic	Deutsch 450-12-10PN
J11 (Coax)	Bus I/O	SMA or equivalent (75Ω)
J12 (Coax)	Data input	SMA or equivalent (75Ω)
J13 (Coax)	Data output	SMA or equivalent (75Ω)

Table C-3

MODEM CONNECTOR AND SIGNAL LIST

Connector	Signal Name	Pin Number
J10	Power return	H
	-12 volts	A
	Transmitter inhibit	F
	Logic ground	E
	+12 volts	B
	+5 volts	G
	Transmitter power (+28 V)	K
	Carrier on	C

C. 3. 1. 5. 2 Cable Performance Requirements

A. The coaxial cable shall cause no more than 3 db per 100 foot attenuation at 300 MHz with a temperature coefficient of expansion of no more than ±250 ppm.

B. The cable shall attenuate external noise above 1 MHz a minimum of 40 db and above 50 MHz, a minimum of 50 db. Attenuation is with respect to an unshielded wire reference.

C. The cable shall exhibit a nominal characteristic impedance of 75 ohms.

C. 3. 1. 6 Data Bus Terminal (DBT) Functional Characteristics

The Data Bus Terminal shall interface between a 10-MBPS Biphase L (Manchester Type II) coded data bus channel and any one of eight one-MBPS bipolar NRZ coded I/O channels. The DBT shall interface with the data bus through modems as described in C. 3. 1. 4. The modem provided for the breadboard shall operate on a frequency located at 140 MHz and shall be transparent to software. Logic, addressing, and connectors/ports shall be included in the DBT to permit expansion to three 10-MBPS, FDM channels. Each DBT shall respond to a uniquely assigned hardwire-programmable address.

The eight DBT I/O channels shall transfer data and commands sequentially to and from peripheral devices such as RDAU's or experiment subsystems at a one-MBPS rate. The DBT shall have the capability to "read" data from any one of eight channels. It shall also have the capability to "write" commands or data to any specific channel. The DBT shall also recognize a special command for device-to-device transfers, whereby one DBT communicates with another (for example, an experiment-to-tape communication).

C. 3. 1. 6. 1 DBT Primary Performance Characteristics

The DBT shall contain the major functional blocks and registers shown in Figure C-10. Performance of the DBT shall be as indicated by the flow diagram of Figure C-11 in accordance with the format and functional descriptions as contained in the following paragraphs.

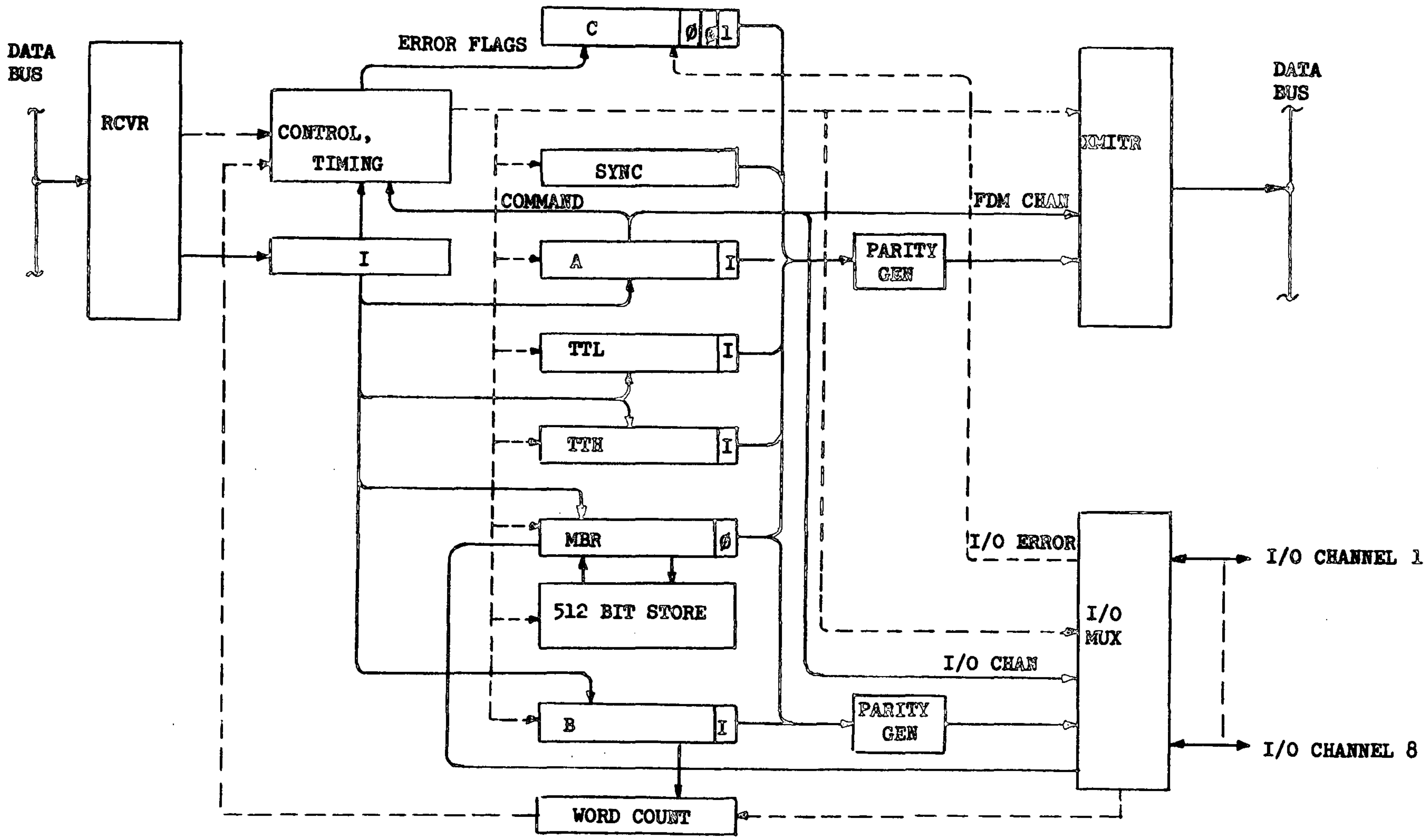


Figure C-10. Data Bus Terminal Block Diagram

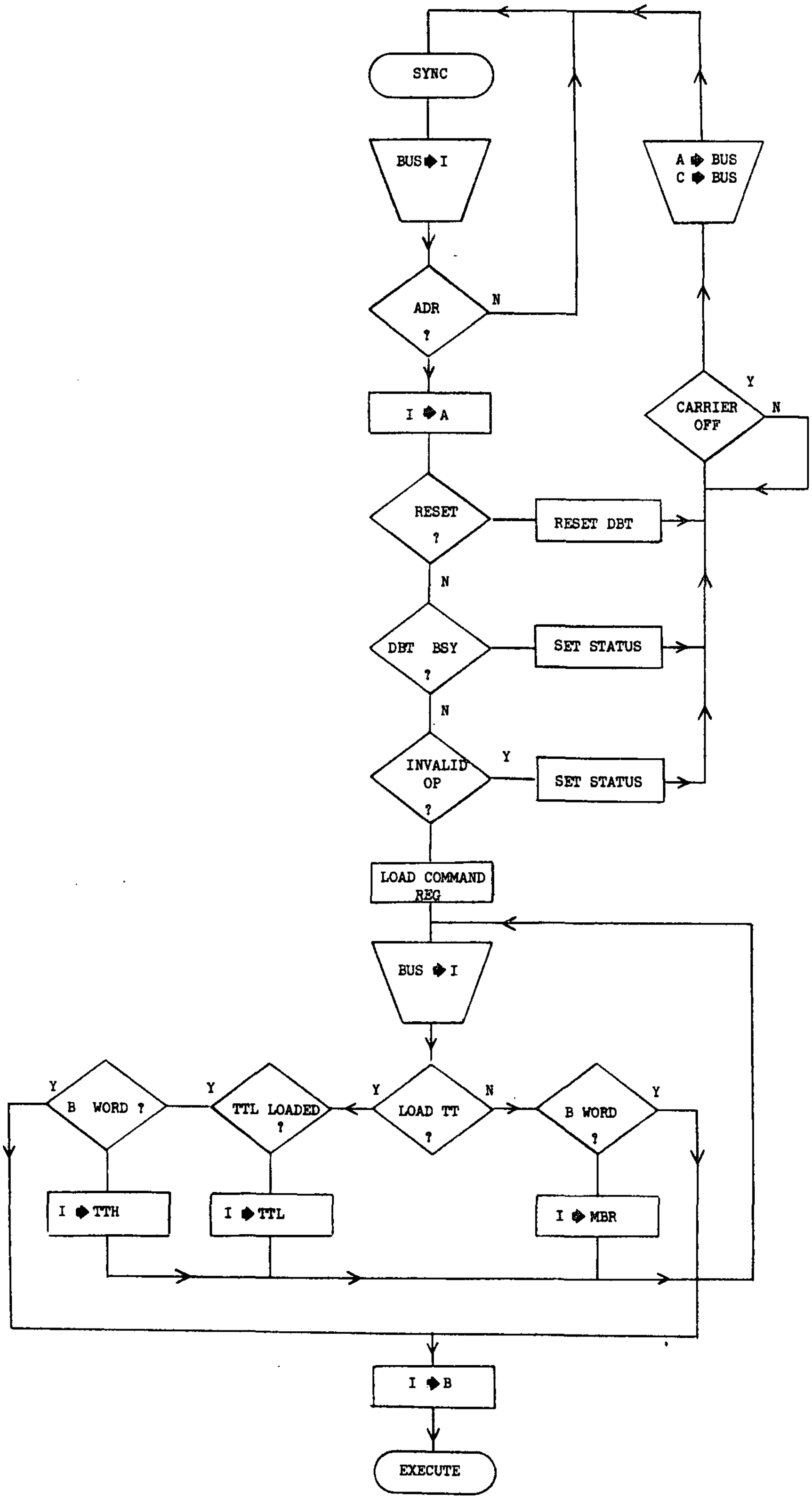


Figure C-11. Data Bus Terminal Flow Diagram

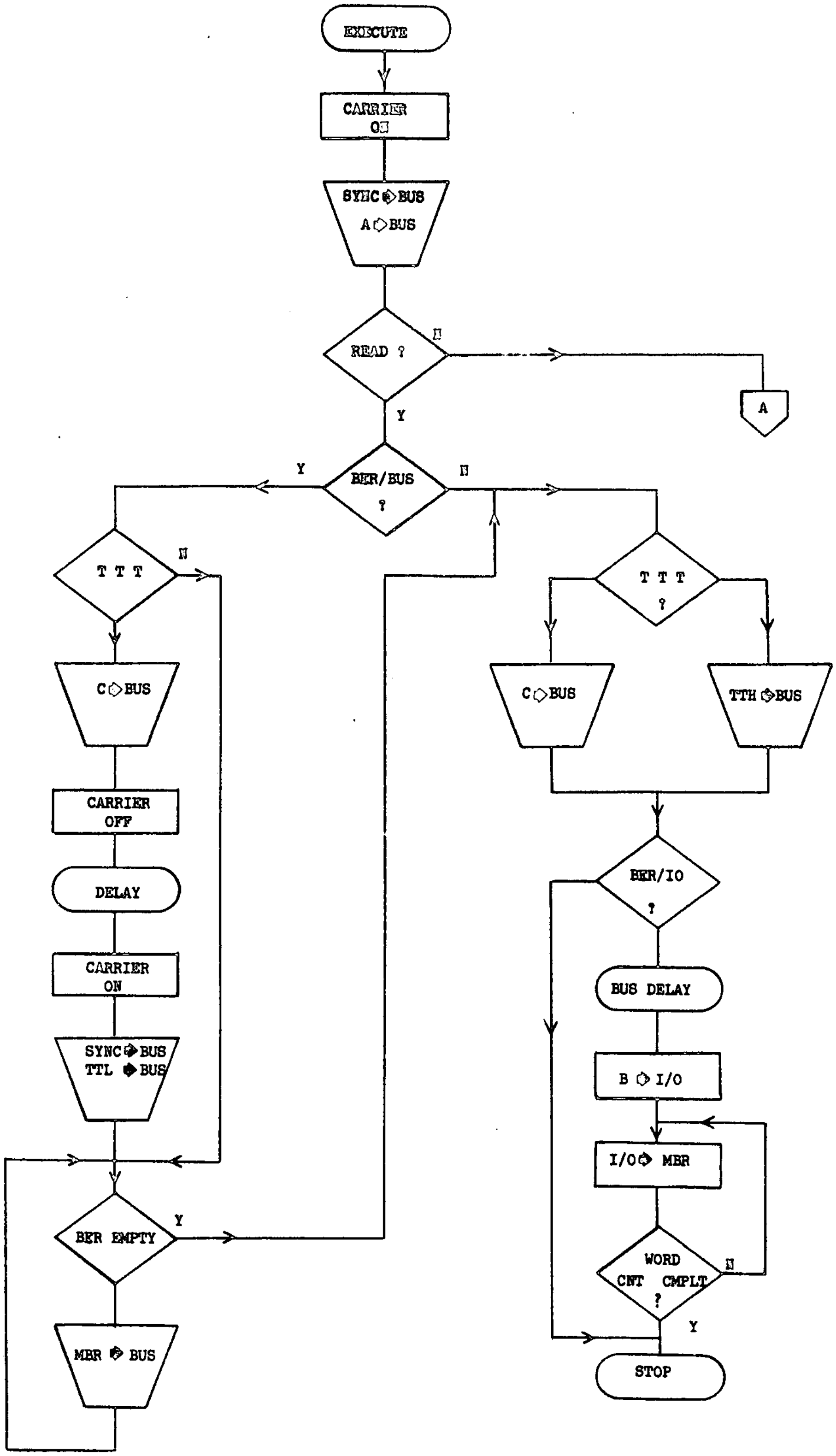


Figure C-11. Data Bus Terminal Flow Diagram (Continued)

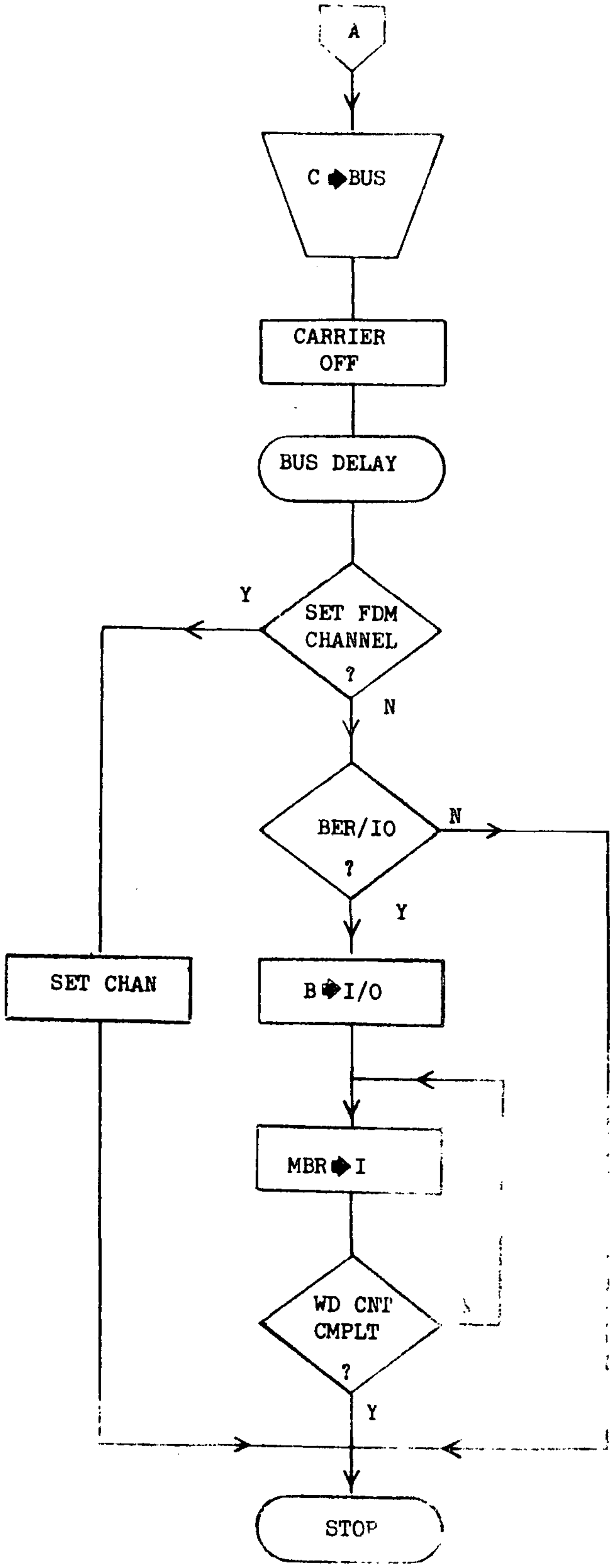


Figure C-11. Data Bus Terminal Flow Diagram (Continued)

C. 3. 1. 6. 1. 1 Operational Control

Each DBT, after recognizing an "A" word following a synch burst, will perform the following functions:

A. Address Decoding—Each DBT shall contain its own unique seven bit address code which shall be programmable by changing a plug-in unit. The "A" word of any command shall contain the address code for a particular DBT in bits 2 to 8. Every DBT on any given FDM channel shall examine any "A" word following a synch burst for its particular address code. Upon recognition of this address code, the DBT shall accept subsequent words for command (function) decoding and data handling. If the address code is invalid, the DBT will discontinue logic decoding until the arrival of another synch burst.

B. Function Decoding—Every "A" word also contains a command or function code bits 12 to 16 used to program an alerted DBT to perform a specific function. Functions shall be decoded after a valid address has been received. The set of DBT functions and their operation shall be as described under C. 3. 1. 6. 1. 1. G, DBT Programming.

C. Channel Address and Function Decoding—Each DBT shall control eight I/O channels addressed by bits 9 to 11 in the "A" word. Specific I/O devices shall then be supplied data and/or commands through the DBT. I/O device subchannels and commands shall be contained within the "B" word.

D. Status—Most "self-test" type operations shall be performed by a "wrap-around" technique in conjunction with individual RDAU's connected to specific DBT's. However, every poll of a DBT shall result in a response, and a part of this response shall be DBT status information contained in the "C" word. Assignment of these status bits shall be as shown in Figure C-12.

E. Word Count Decoding—The word count field in the "B" word shall denote word counts of 1 to 32 words. An instruction shall be recognized by the DBT to denote a zero word message.

F. Parity—The DBT shall check and generate add parity on 18 bits at all interfaces; i. e., DBT to RDAU/subsystem and DBT to data bus.

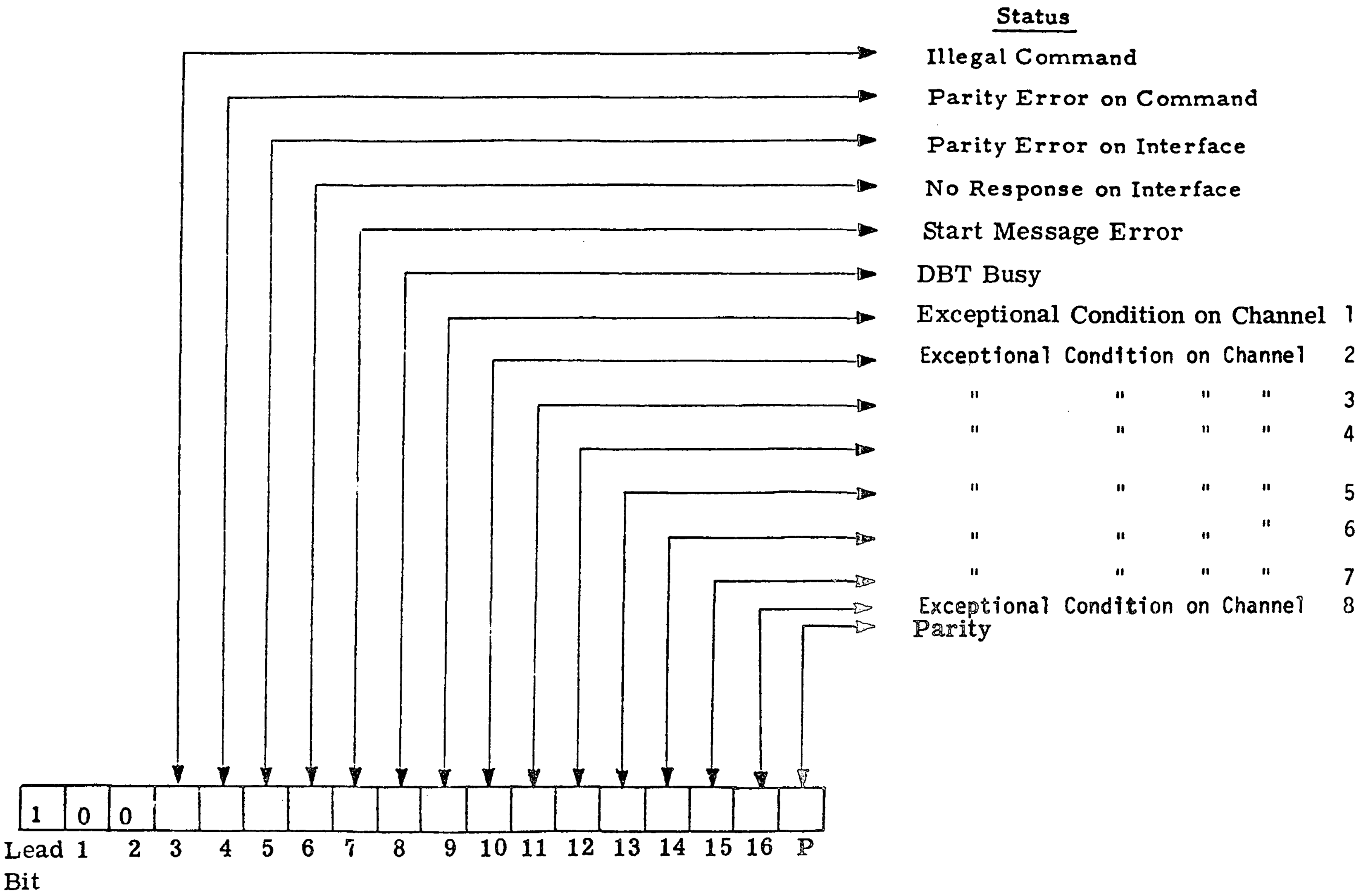


Figure C-12. C Word Format

G. DBT Programming—The following is a specification of the DBT command structure and a description of the valid commands and their operation.

The DBT command field shall consist of five bits, each with its own particular significance as illustrated in Figure C-13.

The valid DBT operations, which shall be defined in Figure C-13, are described below:

1. 11111—RESET DBT
2. 10000—LOAD TTT REG.
3. 10010—SET FDM CHANNEL
4. 00000—NO OP
5. 00101—READ I/O TO BUFFER
6. 0X110—READ BUFFER TO BUS
7. 0X111—READ BUFFER TO BUS AND I/O TO BUFFER
   A 1 in position X above will result in the operations being performed as a TT transfer.
8. 00100—NO OP
9. 00001—WRITE BUFFER TO I/O
10. 00010—WRITE BUS TO BUFFER
11. 00011—WRITE BUS TO BUFFER AND BUFFER TO I/O
12. 10001—CONTROL I/O

The DBT operations associated with each command are as follows:

1. RESET DBT—This command has highest priority and shall cause any operation in process to stop and resets the TTH, TTL, and C registers.
2. LOAD TTT REG. —In this command, the two data words from the bus shall be loaded into the TTL and TTH registers. These registers shall be cleared by loading all 0's on receipt of the reset command.
3. SET FDM CHANNEL—This command allows a DBT to be reassigned to a different FDM channel. The DBT response shall be an "A" word and a "C" word transmitted on the previously assigned channel frequency. Following the

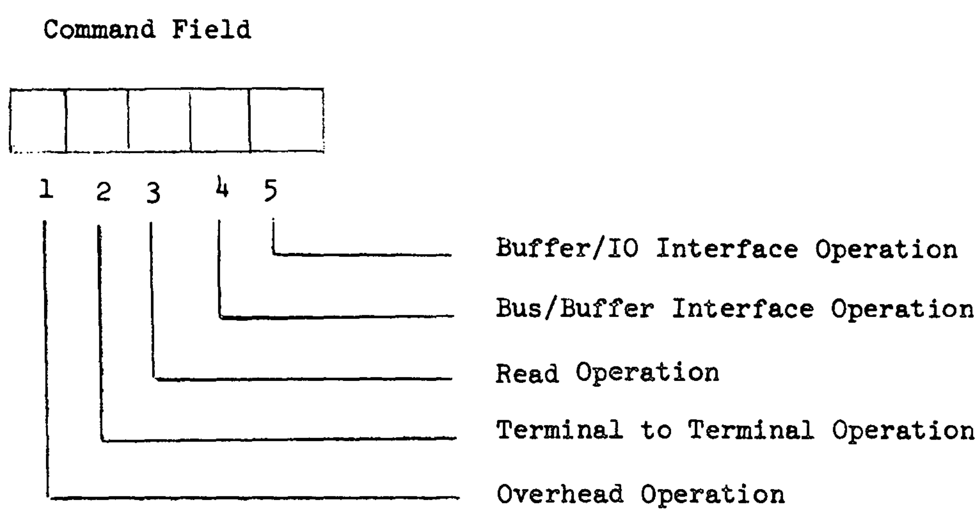


Figure C-13. Command Field

response, the DBT will switch to the new frequency. Since the IMS breadboard model will contain but one FDM channel, all associated logic controls will be performed, but all codes will select the same frequency.

4. NO OP—This command causes the "A" and "B" registers to be loaded. The DBT responds with an "A" and a "C" word, but no other operation is performed.
5. READ I/O TO BUFFER—This command shall be received as an "A" and a "B" word from the bus. Immediately following address and command decoding, a "response" shall be sent over the bus, consisting of the original commanded "A" word followed by a "C" word. Once the command has been received and the response sent, execution of the command shall begin after an 8-μsec delay. The I/O channel address shall be extracted from the "A" word. The "B" word shall be transmitted over the I/O channel and response data received back. The number of received data words shall correspond to the number specified in the count field, bits 2 to 7, of the "B" word. The data are loaded into buffer storage.
6. READ BUFFER TO BUS—In order to access the buffer, this command may be sent which shall then cause the contents of the buffer storage to be transmitted onto the data bus as data words. These words shall appear, in time, between the response "A" word and the "C" word. No further action following transmission of the status word shall take place in the DBT.
7. READ BUFFER TO BUS AND I/O TO BUFFER—Operation of this command is a sequence of commands 5 and 6. The buffer shall be transmitted to the bus per command 6, but following the "C" word transmission, the I/O channel shall be read into the buffer per command 5.
8. NO OP—Identical to command 4.
9. WRITE BUFFER TO I/O—This command causes the contents of the buffer to be transferred to the specified I/O channel.

C. 3. 1. 6. 1. 2 PCM Format and Bit Synchronization

All data on the data bus shall be in a biphase L code as defined in Telemetry Standards Document 106-66. Each message shall be preceded by a sync burst which consists of 13 zeros followed by 101 (i. e., 0000000000000101). During the sync burst, the modem and DBT data clock synchronization circuits shall be initialized. Clock synchronization shall be generated by the DBT.

C. 3. 1. 6. 1. 3 Error Flags

Error flags shall be indicated by a logic one in the "C" word in bit positions defined in Figure C-12. Terminal time out indicated by the "no response on interface" flag will result if any RDAU or other device fails to respond within 1 millisecond.

C. 3. 1. 6. 1. 4 Buffer

The buffer storage shall be a sequential access 512 bit semiconductor memory. The buffer shall operate at 10 MBPS when interfacing with the data bus and at 1 MBPS when interfacing with the I/O channel interface.

C. 3. 1. 6. 1. 5 Component Test

DBT testing shall require software diagnostic routines, as a simple "wrap-around" is not practical for the DBT alone. Fault isolation to the DBT shall be possible, however. A capability shall also be provided for single-stepping the clock input while reading in instructions and data as a troubleshooting aid.

C. 3. 1. 6. 1. 6 RDAU I/O Channel Interface

The DBT shall provide 8 1-MBPS serial digital interfaces for communication with RDAU's or other devices. Each interface shall be made through three twisted shielded wire pair cables. One cable shall contain a continuous 1-MBPS clock output which also provides a message start signal from the DBT. A second cable shall provide the DBT serial bipolar NRZ formatted data output. The third cable shall be a serial bipolar NRZ formatted data input. The DBT when interfacing with an RDAU or other device shall be capable of providing a dc isolated, transformer-coupled interface.

Figure C-14 shows the interconnection, and Figure C-15 defines the bipolar NRZ format. Requirements for the three signals of each interface are described in the following paragraphs. All specified voltages are differentially measured between the LO and HIGH signal lines of the respective wire pairs inputs. Nominal line impedance shall be 70 ohms ±20 percent.

C. 3. 1. 6. 1. 6. 1 DBT Clock Output

Each of the eight DBT clock outputs shall provide a transformer-coupled, 1-MBPS, 50-percent duty cycle timing signal which is continuous except when immediately preceding the start of a message. As shown in Figure C-15, a clock shall be inhibited to signify the start of a message. Characteristics of the clock signal are as follows:

A. Output Levels—The peak-to-peak output voltage of the clock driver shall be 3.4 ± 0.6 volts.
B. Output Impedance—The output impedance shall be 70 ohms ± 35 ohms.
C. Waveform—The line-to-line differentially measured rise and fall times, measured between the 10- and 90-percent amplitude points, when driving into a 70 ohm ± 20 percent resistive load, shall be less than 100 nsec. Signal droop shall be less than 10 percent.
D. Frequency—The frequency of the clock, disregarding the missing clock message sync, shall be 1 MBPS ± 0.1 percent.
E. Duty Cycle—The differentially measured (line to line) clock duty cycle shall be 50 percent ± 3 percent.
F. Short Circuit Protection—A line-to-line or line-to-ground short circuit shall not cause permanent damage to the clock driver circuit.

C. 3. 1. 6. 1. 6. 2 DBT Data Output Signals

Each of the eight DBT data outputs shall provide bipolar NRZ-formatted, transformer-coupled, balanced outputs. Figure C-15 shows a typical formatted message. Output levels, impedances, and waveforms shall be as specified in C. 3. 1. 6. 1. 6. 1 for the DBT clock. Other DBT data output characteristics shall be as follows.

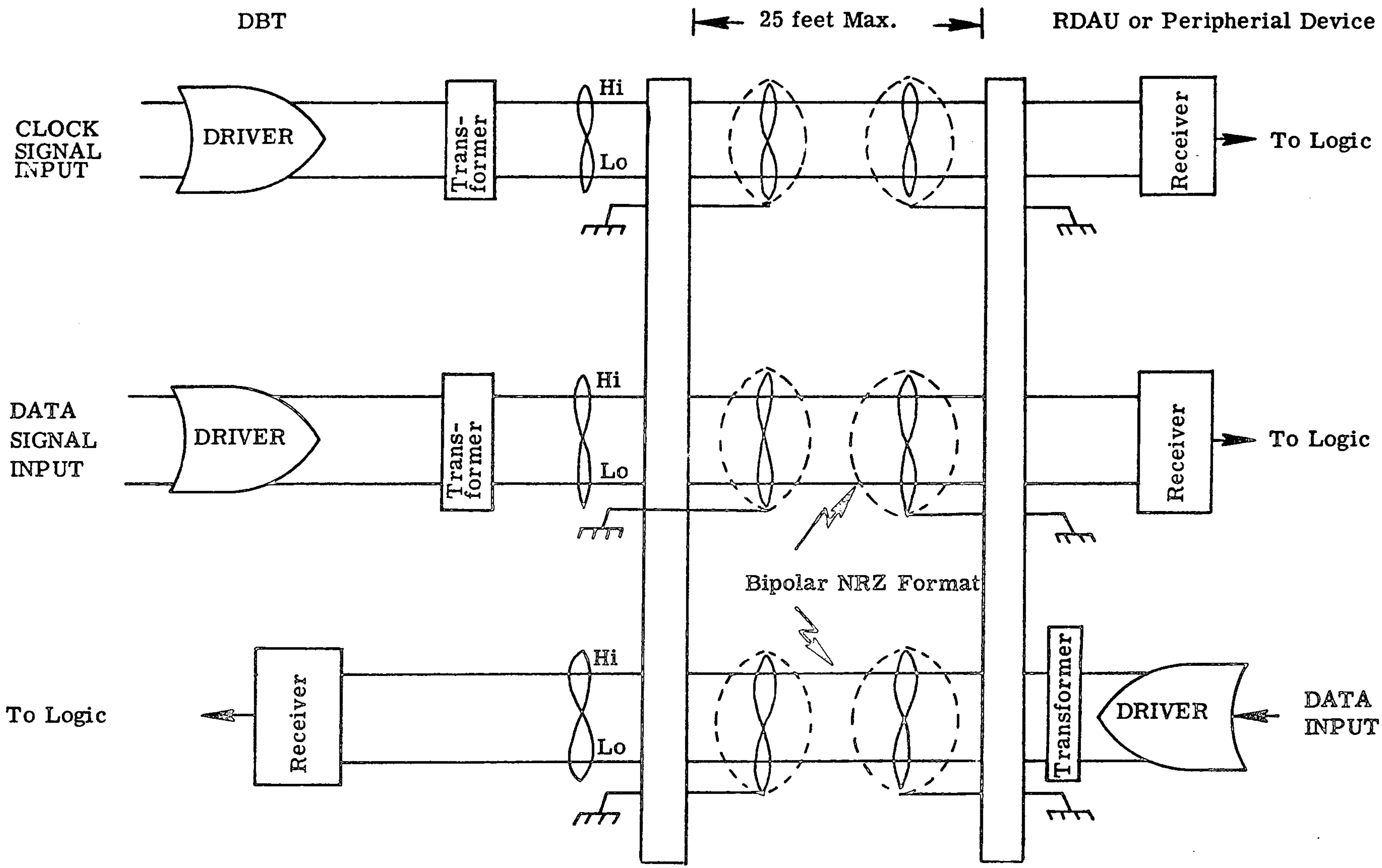


Figure C-14. DBT to RDAU/IO Channel Interface

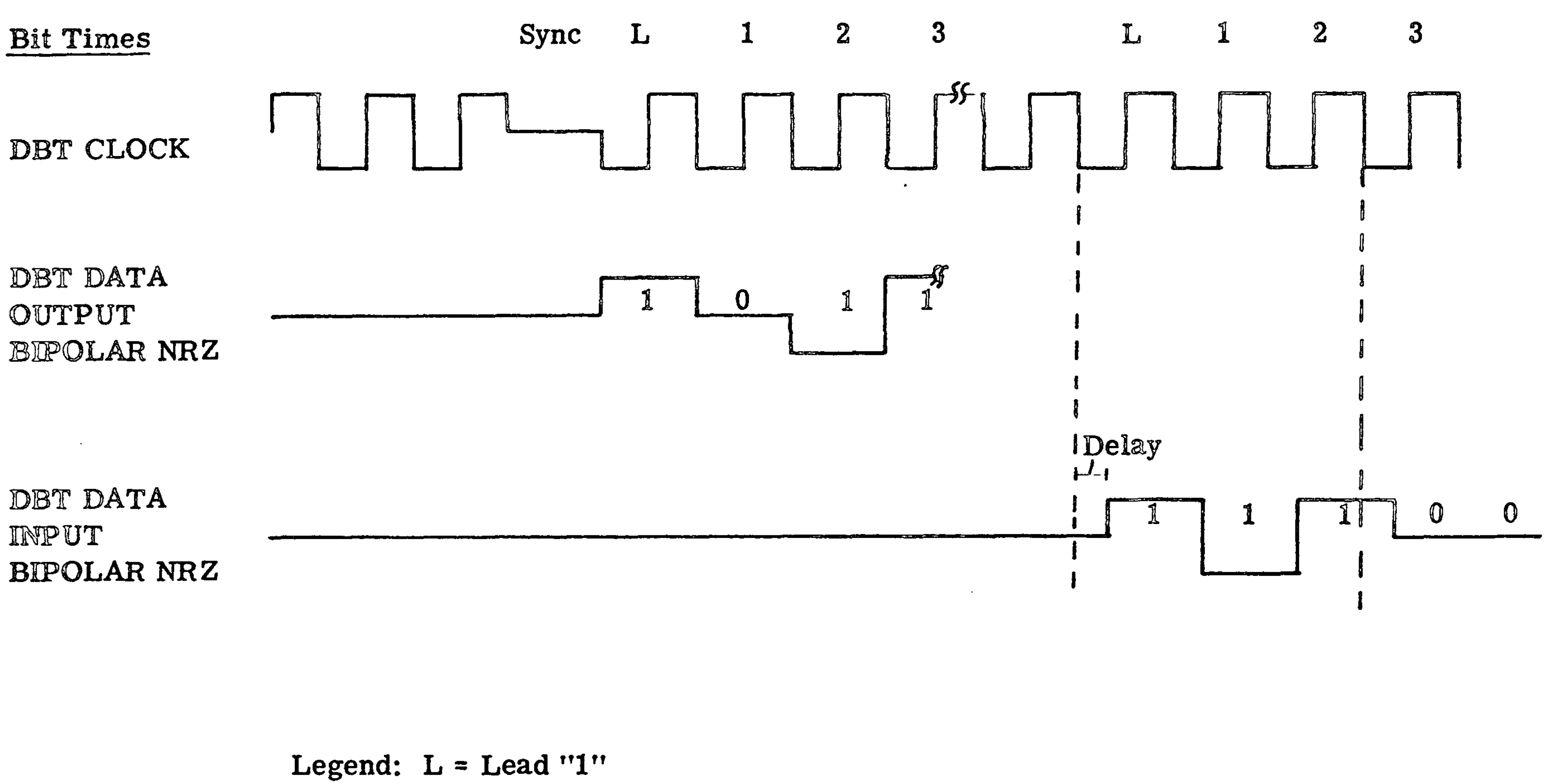


Figure C-15. RDAU/IO Channel Signal Definition

The DBT shall respond to the bus with an "A" and a "C" word, wait for 8 microseconds, and transfer the "B" word to the I/O channel, followed by the buffer contents. The number of data words transferred to the I/O channel shall be specified by the count field of the "B" word.

10. WRITE BUS TO BUFFER—This command causes data words from the bus to be written into the buffer. Presence of the "B" word signifies the end of data. The DBT will respond with an "A" and a "C" word after receipt of the "B" word.

11. WRITE BUS TO BUFFER AND BUFFER TO I/O—This command is a combination of commands 10 and 9, where the buffer is fielded per command 10, then transferred to the specified I/O channel per command 9.

12. CONTROL I/O—This command shall cause the "B" word from the bus to be transferred over the I/O carrier selected in the normal manner. No transfer of data words is assumed with this command in either direction.

13. TERMINAL TO TERMINAL TRANSFER—Terminal-to-terminal transfer shall be a special case of the previous "read" commands. Identical operations to those described shall occur, except that the DBT will make two transmissions where the contents of the TT registers shall be used to preface the second DBT response. The TT registers shall contain the address of another DBT and some "write" command, as an A' and B' word. The first response is a normal synch "A" and "C" word transmission. The second response occurs after a nominal delay and consists of a synch, A' word, up to 32 data words, and a B' word. The second DBT shall recognize its address and proceed to act on the following data as if it had been transmitted by the BIU.

A. Format—The output shall be in a bipolar NRZ format. Both lines shall be in a logic zero state when no data are being transmitted.

B. Phasing—The center of a logic-one pulse as measured half way between the 50 percent points of the rise and fall transitions shall be in coincidence with the 50 percent point of the rising edge of the clock to within 40 nsec.

C. Short Circuit Protection—A line-to-line or line-to-ground short circuit shall not cause permanent damage to the data driver circuit.

C. 3. 1. 6. 1. 6. 3 DBT Data Input Signals

The eight data inputs shall be received by the DBT. Input signals shall be in a bipolar NRZ format as defined in Figure C-15. The DBT data inputs shall have the following characteristics:

A. Input Impedance—The line-to-line input impedance while receiving a steady state logic one or logic zero shall be 70 ± 20 ohms.

B. Input Thresholds—A line-to-line 1-microsecond pulse input of greater than 1.0 volts shall be interpreted as a logic one. A differential input signal of less than 0.4 volts shall be received as a logic zero. Both levels measured at the receiver.

C. Common Mode Rejection—The receiver shall be insensitive to common mode signals of 5 volts peak-to-peak over the frequency range of dc to 5 MHz.

D. Phasing—The DBT shall accept input signals that are delayed relative to the falling edge after DBT clock output by 800 ± 150 microseconds.

E. Limit Check Signal—The DBT shall recognize a single microsecond pulse of either polarity on any input data lines as an indication that an out-of-limits condition exists in an RDAU and set the appropriate flag in the "C" register.

C. 3. 1. 6. 1. 6. 4 Terminal Connector Assignment

The connector assignment for the terminal shall be as shown in Table C-4. Pin functions shall be as shown in Table C-5.

Table C-4

DBT CONNECTOR ASSIGNMENT

Designation	Name	Part Number
J1	Terminal I/O	Deutsch 450-14-15PN
J2	Terminal I/O	Deutsch 450-14-15PW
J3	Terminal I/O	Deutsch 450-14-15PX
J4	Terminal I/O	Deutsch 450-14-15PY
J5	Terminal I/O	Deutsch 450-14-15SN
J6	Terminal I/O	Deutsch 450-14-15SW
J7	Terminal I/O	Deutsch 450-14-15SX
J8	Terminal I/O	Deutsch 450-14-15SY
J9	115 V power	Standard Receptacle
J10	Power and logic	SMA or equivalent (75Ω)
J12 (Coax)	Data output	SMA or equivalent (75Ω)
J13 (Coax)	Data input	SMA or equivalent (75Ω)

C. 3. 1. 6. 2 DBT Secondary Performance Characteristics

C. 3. 1. 6. 2. 1 Prime Power

The DBT shall operate from standard single-phase 115 vac (RMS) plus 15 or minus 10 volts, 60 Hz, plus or minus 1. 5 Hz power. Input power shall be less than 75 watts.

C. 3. 1. 6. 2. 2 Environment

The DBT shall be designed to operate in a laboratory environment under the following conditions:

A. Ambient Temperature—10°C to 50°C.

B. Barometric Pressure—Sea level to 5, 000 feet.

C. Relative Humidity—10 to 80 percent.

C. 3. 1. 6. 2. 3 Mechanical

The DBT shall be designed for mounting in a MIL-STD-189, 19-in. equipment rack. Nominal dimensions are 19 by 23 by 3. 5 in. Weight shall be less than 30 pounds. Connectors shall be accessible from the rear. No special cooling shall be required.

Table C-5

DBT CONNECTOR AND SIGNAL LIST

Connector	Signal Name	Pin Number
J1-J8	Clock +	A
	Clock -	B
	Clock shield	C
	Data out high	D
	Data out lo	E
	Data out shield	F
	Data in hi	H
	Data in lo	J
	Data in shield	K
	Chassis ground	G
J9	115 volts	1
	115 volts	2
	Ground	3
J10	Power return	1
	-15 volts	3
	Transmitter inhibit	5
	Logic ground	6
	+15 volts	15
	+5 volts	17
	Transmitter power (+15 V)	19
	Carrier on	20

C.3.1.6.2.4 Isolation

Isolation between the signal and chassis ground shall be greater than or equal to 2 megohms at 25 vdc.

C. 3. 1. 6. 3 Operability

C. 3. 1. 6. 3. 1 Reliability—Not applicable.

C. 3. 1. 6. 3. 2 Maintainability—TBD.

C. 3. 1. 6. 4 Quality Assurance—TBD.

C. 3. 1. 7 RDAU Functional Characteristics

Remote data acquisition devices (RDAU's) shall interface with data bus terminals. They shall be capable of acquiring individual data channels, multiple data channels (frames), performing limit checking, and providing discrete commands to other devices.

Figure C-16 contains a block diagram of the device showing the manner in which the function shall be implemented. It includes input and output buffers for transferring data in and out of the unit, instruction logic for defining one of 16 possible operation modes, an output decoder for command address decoding, an address counter for sequencing through memory or data channels, analog and digital gates with an associated analog-to-digital converter, and circuitry associated with limit-check functions.

C. 3. 1. 7. 1 RDAU Performance Characteristics

RDAU's shall accept 16-bit instruction and data words in a serial format with a 1-MBPS clock. Commands will then be decoded and the requisite action performed. Specific performance requirements are contained in the following paragraphs.

C. 3. 1. 7. 1. 1 Control Logic

The RDAU shall contain control logic for accepting, decoding, and performing control functions. Table C-6 contains a list of instruction codes and their associated control functions. The flow diagram of Figure C-17 indicates the sequence of operations which follow the receipt of each instruction. In the event a parity check fails on any instruction, the unit will return to its initial state, the operation called for by the instruction will not be performed.

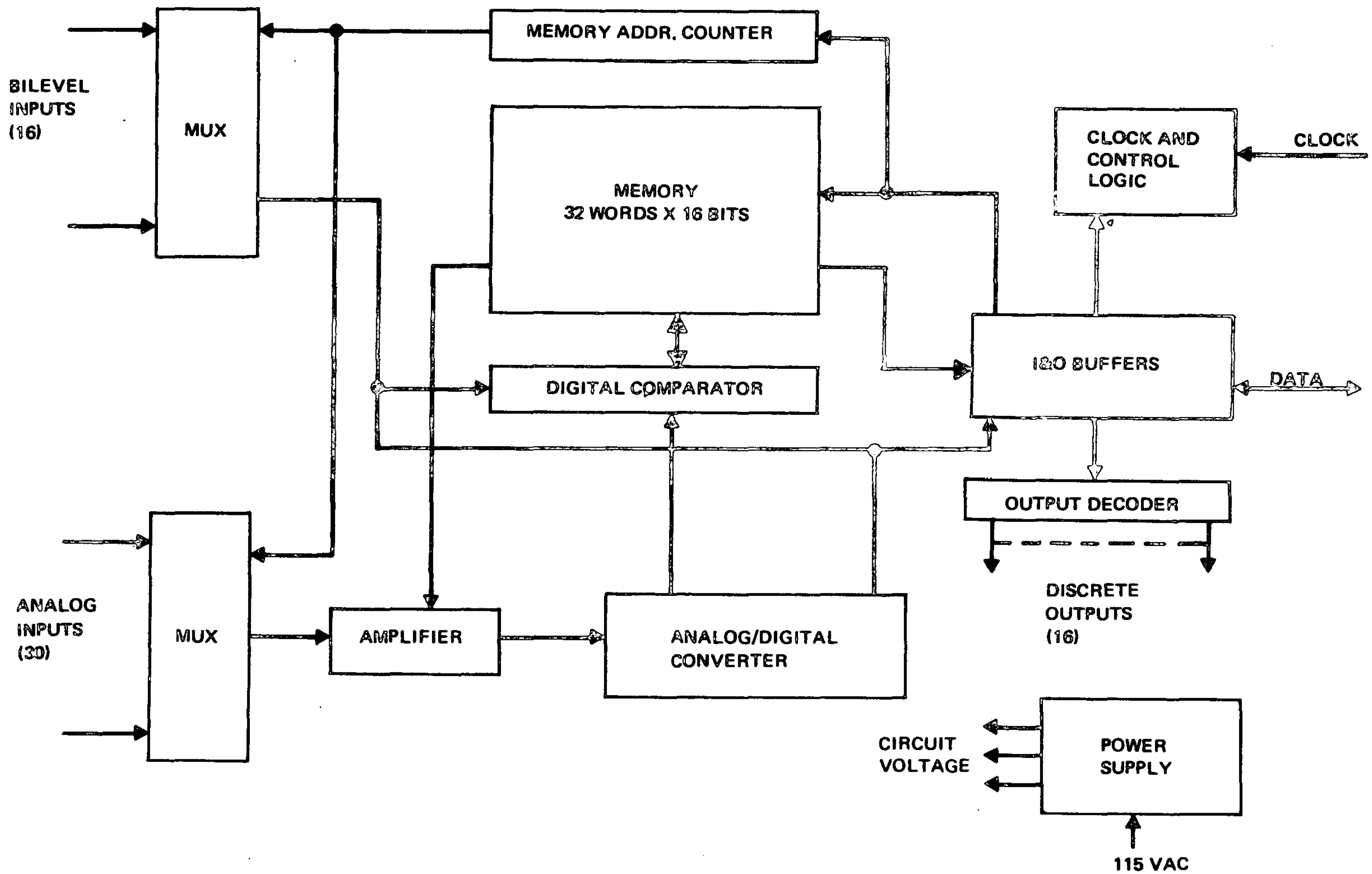


Figure C-16. Remote Data Aquisition Unit

Table C-6

INSTRUCTION CODES

Code (1234)	Function
0000	No operation (NOP)
0001	Read limit channel (RLC)
0010	Read limit memory (RLM)
0011	Read data frame (RDF)
0100	Read data channel (RDC)
0101	Read out-of-limit status (ROL)
0110	Spare
0111	Test
1000	Load limit channel (LLC)
1001	Load limit memory (LLM)
1010	Command (CMD) "ON"
1011	Command (CMD) "OFF"
1100	Enable limit check (ELC)
1011-1111	Spare

The RDAU will then wait for the next instruction. All functions requiring a response to the data bus terminal shall initiate data transfer in a time period not to exceed 14 microseconds.

C. 3. 1. 7. 1. 2 Input/Output Response Rate

The maximum period between receipt of the last instruction bit to the first bit of data output to the terminal shall be as follows:

Instruction	Response Time (microseconds)
Read Limit Channel	4
Read Limit Memory	4
Read Data Frame	14
Read Data Channel	14
Read Out-of-Limit Status	4
Test	14

The above is predicated on a clock rate of 1 MBPS.

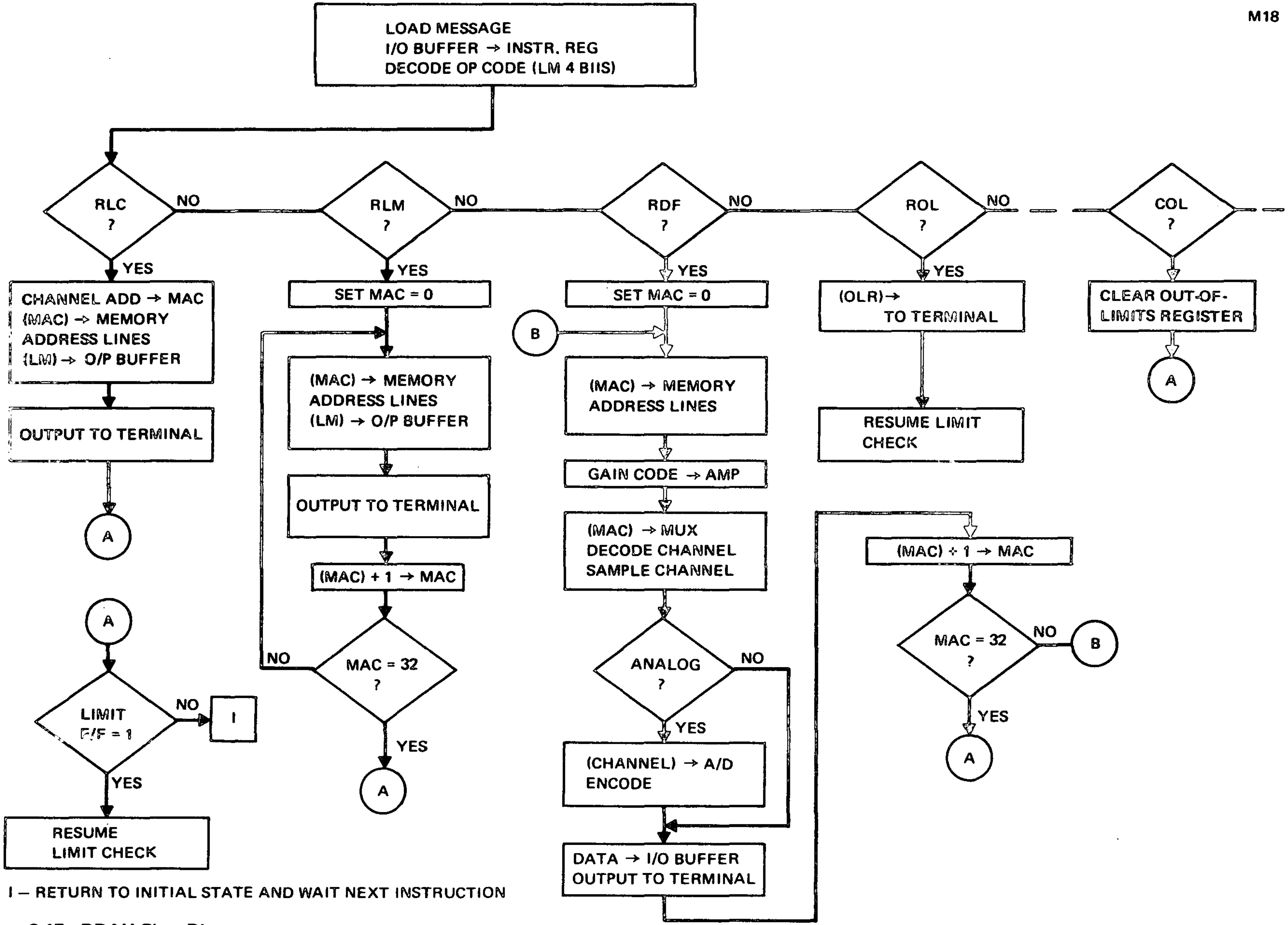


Figure C-17. RDAU Flow Diagram

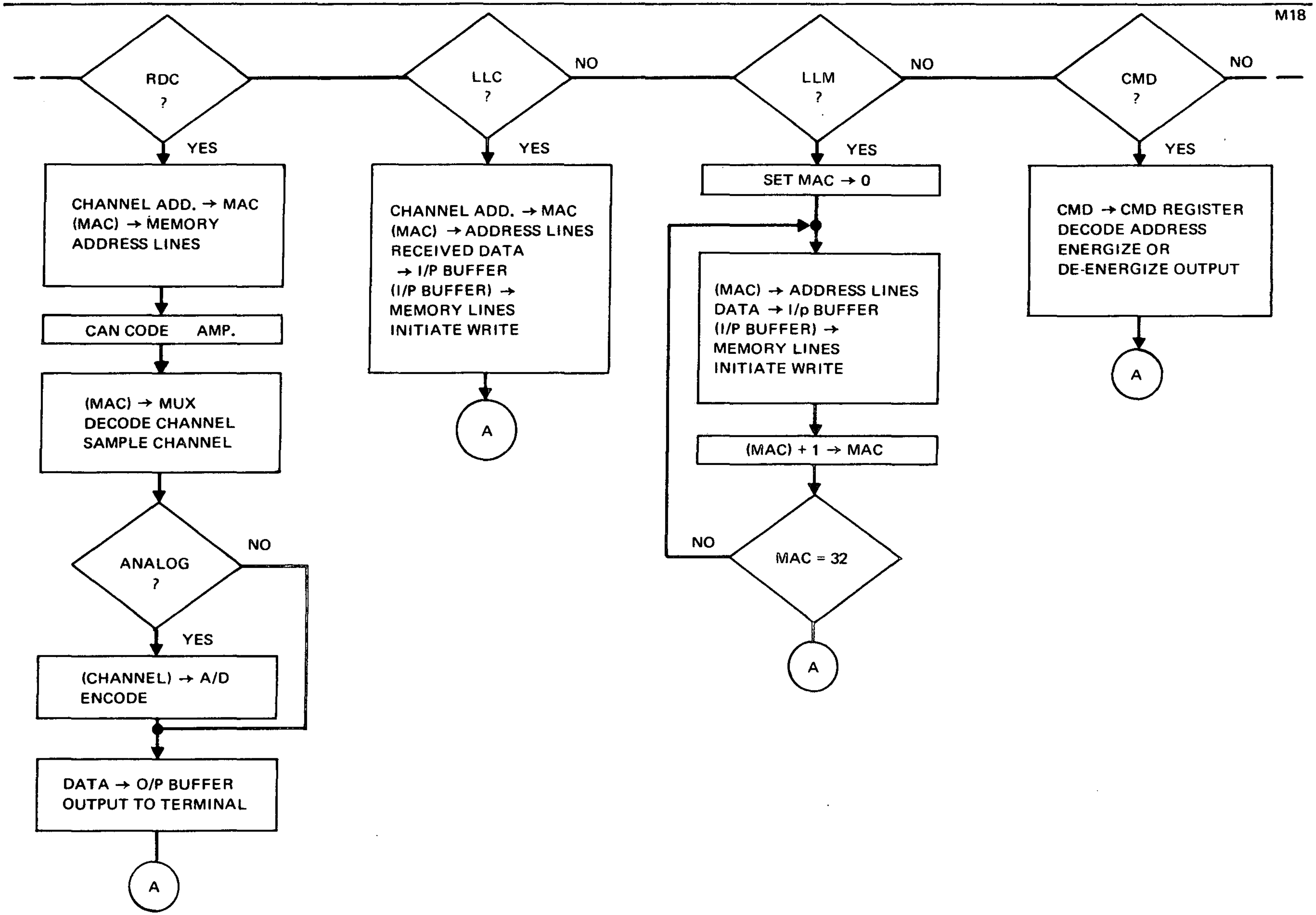


Figure C-17. RDAU Flow Diagram (Continued)

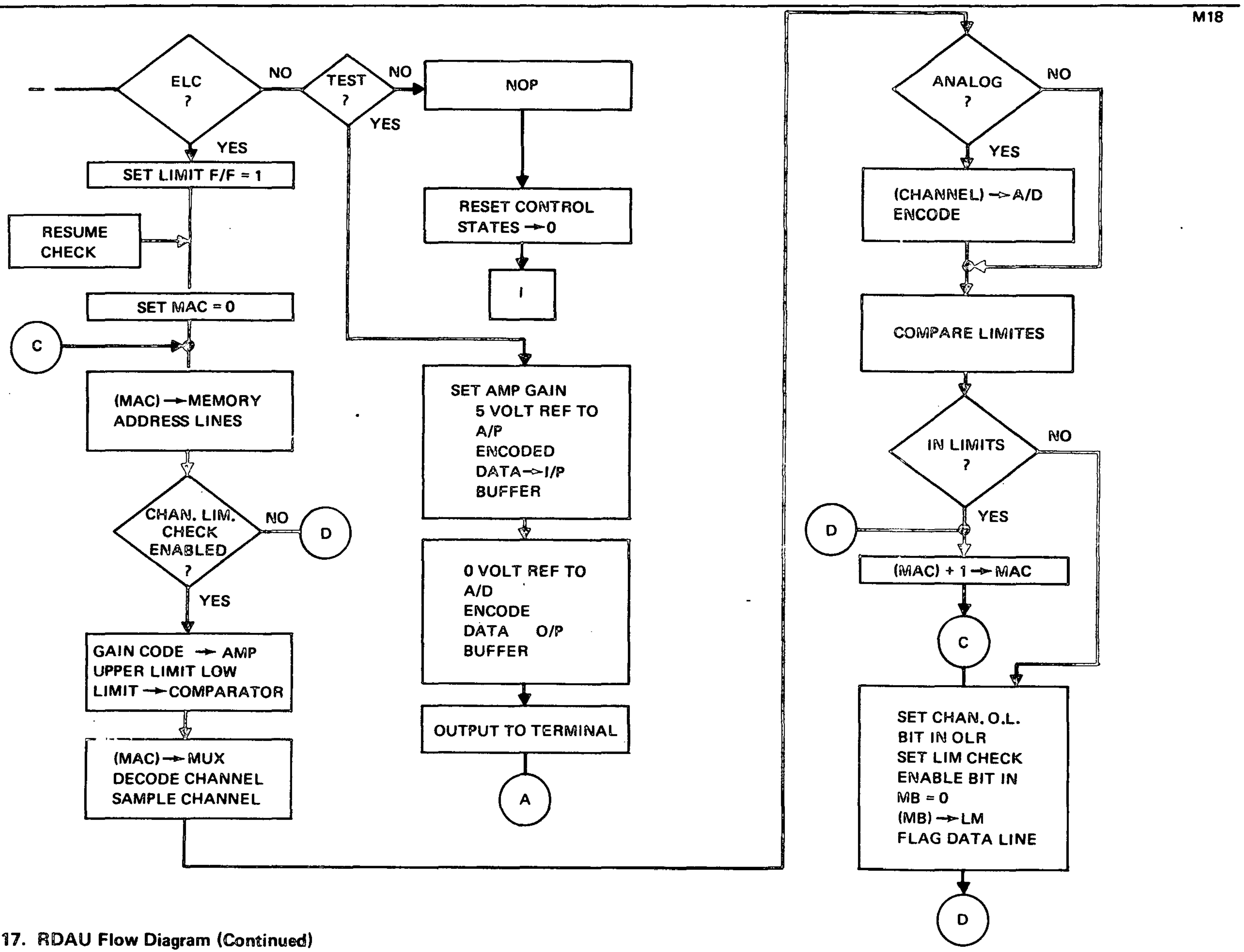


Figure C-17. RDAU Flow Diagram (Continued)

3

C. 3. 1. 7. 1. 3 Format Characteristics

The formats for words input and output between terminals and RDAU's shall be 18 bits in length, including a lead one or zero and a parity check bit. Data shall be transferred, most significant bit first, and parity check shall be odd. Input data to the RDAU's from the terminals shall consist of a single instruction ("B" word) or an instruction followed by a message consisting of 1 or 32 data words. Output responses shall be 1, 3, 16, or 32 words in length. The number of words in a transfer shall be directly related to a particular instruction, allowing the derivation of a message word count. All transfers shall be continuous; i. e., no gaps between words.

The format for instructions or commands consists of a "B" word as shown:

<u>Instruction Format ("B" Word)</u>

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	1	0	1	INSTR				Word Count					Address					P

Bit 0: Command Word (Lead 1)
Bit 1: Not an A Word
Bit 2: B Word
Bit 17: Parity

Bit position "0" provides an indication that an instruction has been received. Bit positions "1" and "2" may be disregarded since they serve no RDAU function, but are included only to allow the terminal to perform as a transparent device to inputs and outputs.

The message format following the instructions "load limit channel" or "load limit memory" shall be as shown:

<u>Message Format (General)</u>

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	0	Message																P

Bit 0: Lead "0"
Bit 17: Parity Bit

The lead "0" differentiates between an instruction and a message word. The message will contain data for one or all channels (as indicated by the instruction) of the memory (memory map shown in Table C-7). Receipt and decoding of the load limit channel instruction will indicate one message word is to follow. The load limit memory instruction will indicate that 32 message words are to follow. The message word following a load limit channel instruction shall begin with column bit position "0". The load limit memory instruction shall begin with column/row bit position "0," and rows shall be read in sequentially.

The general format for response to an instruction is as shown:

Response Format (General)

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	1	Data																P
	Lead "1"																	Parity

The response to a read limit channel instruction shall be a transfer of one row of the limit memory beginning with column bit position "0" as shown in Table C-3. The response to read limit memory instruction shall be a transfer of the entire memory contents beginning with row/column bit position "0" with rows readout sequentially.

The response to the read data frame instruction shall be a sequential transfer of analog channels 1 through 30 and discrete channels 1 through 16. Digital values will be transferred two to a word for analog channels, and 16 to a word for discrete channels for a total of 16 words.

The format for response to the read data channel instruction will consist of the eight bit digital value of the requested channel after the lead "1" followed by the digital value of the next channel or eight bilevel bits, and a parity bit. Channel address 31 shall not be used. Channel address 30 shall

Table C-7

MEMORY MAP

Row	Column (4) 2,3,4,5,6,7,8	(4) 9,10,11,12,13,14,15	0,	1	Channel
0	Upper limit	Lower limit	E(1)	G(2)	Analog 1
1	Upper limit	Lower limit	E	G	Analog 2
2	Upper limit	Lower limit			Analog 3
3	Upper limit	Lower limit			Analog 4
4	Upper limit	Lower limit			Analog 5
5	Upper limit	Lower limit			Analog 6
6	Upper limit	Lower limit			Analog 7
7	Upper limit	Lower limit			Analog 8
8	Upper limit	Lower limit			Analog 9
9	Upper limit	Lower limit			Analog 10
10	Upper limit	Lower limit			Analog 11
11	Upper limit	Lower limit			Analog 12
12	Upper limit	Lower limit			Analog 13
13	Upper limit	Lower limit			Analog 14
14	Upper limit	Lower limit			Analog 15
15	Upper limit	Lower limit			Analog 16
16	Upper limit	Lower limit			Analog 17
17	Upper limit	Lower limit			Analog 18
18	Upper limit	Lower limit			Analog 19
19	Upper limit	Lower limit			Analog 20
20	Upper limit	Lower limit			Analog 21
21	Upper limit	Lower limit			Analog 22
22	Upper limit	Lower limit			Analog 23
23	Upper limit	Lower limit			Analog 24
24	Upper limit	Lower limit			Analog 25
25	Upper limit	Lower limit			Analog 26
26	Upper limit	Lower limit			Analog 27
27	Upper limit	Lower limit			Analog 28
28	Upper limit	Lower limit	E	G	Analog 29
29	Upper limit	Lower limit	E	G	Analog 30
30	E3,L,E,L,E,L,E	L,E,L,E,L,E,L,	E,	L	Discrete (1-8)
31	E,L,E,L,E,L,E	L,E,L,E,L,E,L,	E,	L	Discrete (9-16)

NOTES:

(1) E—Enable bit (logical "1").
(2) G—Gain bit (logical "1" for low gain, logical "0" for high gain).
(3) L—Limit bit (logical "1" for "on," logical "0" for off).
(4) Most significant bit stored in lowest order row bit position.

provide the 16 bilevel bits. The format for response to the test instruction will provide the eight-bit value of the five-volt reference after the lead "1," followed by the value of the zero-volt reference.

The format in response to the read out-of-limit status instruction shall consist of three data words composed of the limit check enable/disable control bits for 30 analog and 16 bilevel channels beginning with analog channel 1 (bit position 0) and read sequentially. The disabling of the limit check function for any channel by the RDAU will be indicative of an out-of-tolerance condition. Bit 46 shall indicate a format error and bit 47 the status of the RDAU. No response back to the terminal will be required for the enable limit check and the no operation instructions.

C. 3. 1. 7. 1. 4 Data Multiplexing

Analog and digital signals shall be accepted by each unit, amplified, and encoded. All inputs will be double ended or differentially connected to improve noise immunity.

A. Analog/Discrete Channel Capacity—An RDAU shall provide gating for 30 externally connected analog signals and 16 discrete inputs. Failure of any one gate shall not affect more than eight channels. Each digital gate/address shall serialize data from eight individual digital inputs and route this data to the comparator or input/output buffer as appropriate.

B. Command Channel Capacity—An RDAU shall provide command address decoding for 16 discrete outputs.

C. Analog Amplifier—An RDAU shall provide an amplifier with two programmable gains.

D. A/D Conversion—An RDAU shall employ an A/D converter with an encoding rate ≥ 1 MBPS. Each high and low level analog voltage input shall be converted to an eight-bit binary code for serial output, most significant bit first. Bit patterns 00000010 and 11111110 are reserved for negative and positive overvoltages; 00000000, 00000001, and 11111111 shall not be used. Serial outputs from the converter shall be 00000011 to 11111101 corresponding to a high-level analog voltage input from 0.000 ± 0.10 volts to 5.000 ± 0.010 volts, or a low-level input from 0.00 ± 0.08 millivolts to 40 ± 0.08 millivolts.

E. Measurement Accuracy—The end-to-end three sigma error shall be no more than ± the least significant bit for high-level data. The end-to-end 3 sigma error shall be no more than ± the bit preceding the least significant bit for low-level data. (End-to-end is defined as being from gate inputs to A/D converter output.)

C.3.1.7.1.5 Limit Checking

RDAU's shall incorporate a limit check mode which, once initiated, is returned to following all instructions except after receipt of a NO-OP instruction and a parity check error. Although data are encoded to an eight-bit accuracy, high and low limit checking of analog signals shall only be required to seven bits. Discretes will be checked against on or off limits (one or the other but not both). Limit checking shall be performed by a comparator using limits stored in the RDAU memory. Cycle time for a check of all channels shall be less than or equal to 0.10 seconds. Requirements for these devices are as follows:

A. Memory—A memory shall be included in the RDAU's. Memory capacity shall be 512 bits and formated for purposes of loading per Table C-7 of C.3.1.7.1.3. Memory access time shall be $\leq 1.0\ \mu sec$.

B. Comparators—The analog comparator shall simultaneously compare high and low limit values. Both analog and discrete data comparison shall not exceed $8.0\ \mu sec$.

C. Limit Check Signaling—The status of the limit check function shall be made available to the terminal in the following manner:

Upon detection of an out-of-limits channel, the limit check enable bit in the memory shall be set to "0" and a flag raised on the output data lines. The flag shall consist of a 1 microsecond pulse of either polarity (determined by the previous "1" output). Subsequent errors shall not raise a flag until a transfer of the limit check enable status has been requested and completed.

Operation of the RDAU in the limit check mode shall be indicated by bit 47 of the out-of-limits status words.

C. 3. 1. 7. 1. 6 Test

Upon receipt of a test instruction, an appropriate voltage of 5.000 ± 0.005 and 0.000 ± 0.005 shall be sequentially sampled, converted, and output to the terminal.

C. 3. 1. 7. 1. 7 Simultaneous Receipt and Transmission of Data

In the event a new instruction is transmitted prior to completion of the one previously received, the RDAU shall immediately inhibit further translation, return to its initial state, and accept the new message.

C. 3. 1. 7. 1. 8 Parity Error

The detection of a parity error on an input instruction or memory load shall result in nonperformance of the instruction and/or the cessation of the loading operation for the word in error and all following words in the transmission. The RDAU shall return to its initial state and wait for the next instruction.

C. 3. 1. 7. 1. 9 Format Error Indication

A format error shall be shown by a "1" in bit position 46 of the out of limits status words upon the detection of a parity error or the receipt of an instruction prior to completion of a transmission.

C. 3. 1. 7. 1. 10 Component Test

Provisions shall be incorporated to allow single stepping the clock input while reading in instructions as a test and troubleshooting aid. In addition, a suitable display shall be made available on the device which indicates the state of the program, logic/timer, and memory address counter.

C. 3. 1. 7. 2 RDAU Interface Characteristics

The RDAU shall accept a clock and instructions from the data terminal and issue commands to, or acquire analog data from interfacing subsystems.

C. 3. 1. 7. 2. 1 Device Signal Characteristics

The RDAU interface with subsystems shall have the following characteristics.

C. 3. 1. 7. 2. 1. 1 Data Inputs

Data inputs shall be analog signals (maximum frequency of 10 KHz) or discrete voltage levels.

A. Signal Levels — Analog differential voltage levels shall range between 0. 000 ± 0. 005 and 5. 000 ± 0. 005 volts or 0. 000 ± 0. 008 and 40. 000 ± 0. 008 millivolts. Discrete signal levels shall be less than 0. 4 but greater than or equal to -15 volts for off (logical 0) and greater than 2. 4 but less than or equal to 15. 0 volts for an on (logical 1). The direction of amplitude increase shall be positive.

B. Input Impedance

1. Analog channel differential input impedances shall be greater than or equal to 2 megohm resistive, minimum; shunted by 200 picofarads capacitance, maximum; at any time during sampling or nonsampling periods.
2. Bilevel channel input impedances shall be 100 Kohms resistive, minimum; shunted by 100 picofarads capacitance, maximum; at any time except when over voltages are applied.
3. Channel input impedances from either signal line to chassis ground shall be 1 megohm resistive, minimum; shunted by 50 picofarads capacitance, maximum; at any time and the impedance between these signal lines to common signal ground shall be balanced within 20 percent.

C. Overvoltage — Analog and discrete input gates and/or associated circuits shall not be damaged when inadvertently connected to an input voltage less than or equal to ±25 volts. The gate shall recover within fifteen sample times after removal of the fault voltage; i. e., meet stated specifications.

D. Crosstalk — Crosstalk between adjacent channels shall be no greater than that allowed by a leakage impedance between channels of 100 megohms resistive, minimum; shunted by 5 picofarads, maximum.

C. 3. 1. 7. 2. 1. 2 Command Outputs

Command outputs consisting of dc levels shall be provided as follows:

A. Signal Levels — Command outputs shall be 5. 0 ± 0. 5 vdc on and 0. 0 ± 0. 4 off when driving a 1 KΩ load.

B. Pulse Rise and Fall Times — Pulse rise time shall be less than 1 millisecond.

C. Short Circuit Current — Maximum current into a short circuit load shall be limited to 10 ma.

C. 3. 1. 7. 2. 2 Terminal Signal Characteristics

The interface between the RDAU and the terminal shall consist of three twisted shielded cable double-ended signal lines and shall be compatible with the bipolar NRZ DBT I/O channel interface as described in C. 3. 1. 7. 1. 6. Each of the RDAU interface signals (measured with respect to the RDAU signal ground unless otherwise indicated) are as follows:

C. 3. 1. 7. 2. 2. 1 Clock Input

The RDAU shall receive a continuous tristate clock at 1 MBPS with a 50 percent duty cycle from the data bus terminal. The start of a transmission shall be indicated by a transition of the clock to state "B" for one bit time preceding the first data bit. See Figure C-18.

A. Input Impedance — The termination impedance shall be balanced with 39 ± 4 ohms appearing in each line over the frequency range of 0. 1 to 5 MHz. The impedance from either signal line to chassis ground shall be greater than 2 megohms resistive; shunted by 50 picofarads.

B. Input Voltage — The peak differential input signal shall be 3. 4 ± 0. 6 volts with levels of 1. 5 ± 0. 5 volts for state "A", 0. 0 ± 0. 4 for state "B," and -1. 5 ± 0. 5 for state "C".

C. Input Power — The input power on the clock lines shall be greater than or equal to 50 milliwatts but less than or equal to 100 milliwatts.

D. Rise and Fall Time — The clock rise and fall times shall be less than or equal to 0. 125 microseconds between states "B" and "C."

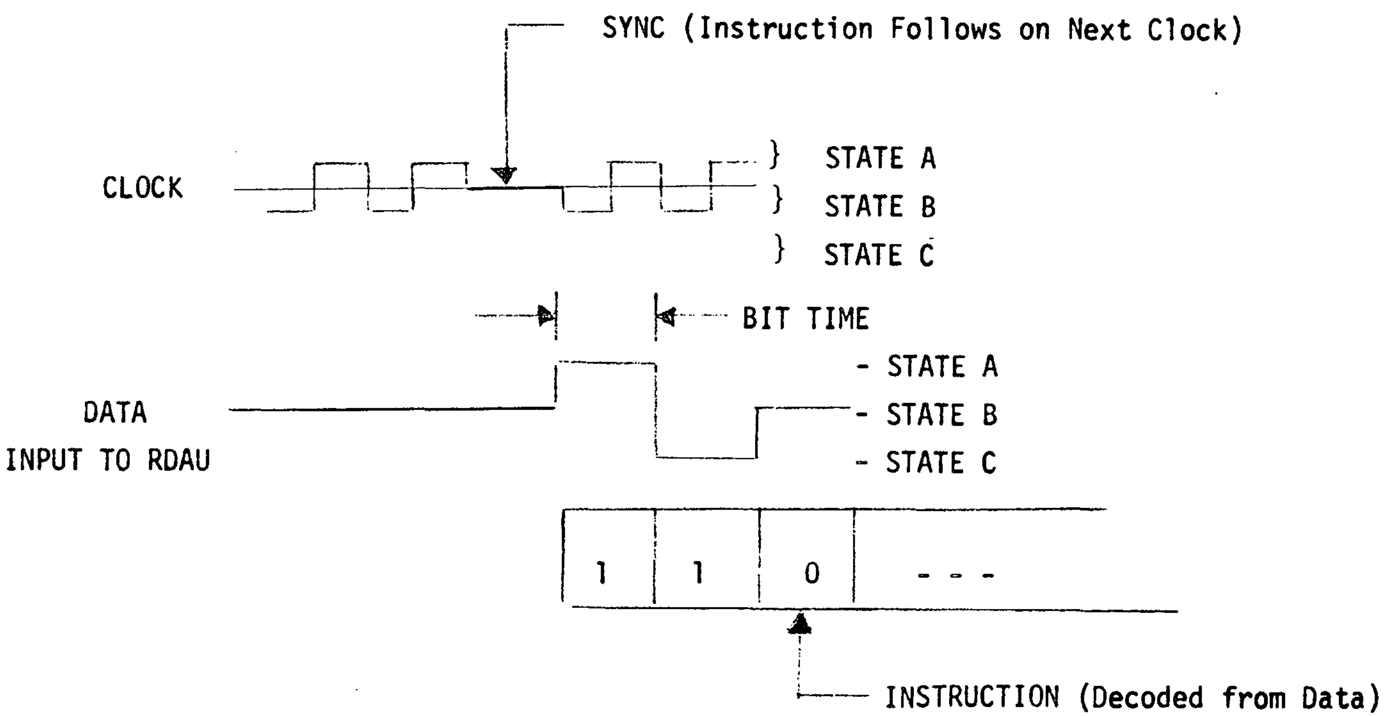


Figure C-18. Clock Wave Form

E. Common Mode Rejection—The receiver shall be insensitive to common mode signals of 5.0 volts or less over the frequency range of dc to 5 MHz.

C.3.1.7.2.2.2 RDAU Data Input

The RDAU shall receive NRZ bipolar data signals at a 1 MBPS rate. Signal characteristics shall be as follows:

A. Input Impedance—Same as C.3.1.6.2.2.1.A.

B. Input Voltage—Same as C.3.1.6.2.2.1.B.

C. Input Power—Same as C.3.1.6.2.2.1.E.

D. Rise and Fall Time—The data rise and fall times shall be less than or equal to 0.25 microseconds between states A and B or C and B.

E. Common Mode Rejection—Same as C.3.1.6.2.2.1.E.

C.3.1.7.2.2.3 RDAU Data Output

The RDAU shall output NRZ bipolar data signals at a 1 MBPS rate. The time delay between the first data bit steady state and the transition of state "B" by received clock pulse shall not exceed 0.425 microseconds. Signal characteristics shall be as follows:

A. Output Impedance—Same as Input Impedance, shown in C.3.1.6.2.2.1.A.

B. Output Voltage—Same as Input Voltage shown in C.3.1.6.2.2.1.B.

C. Output Power—Same as Input Power shown in C.3.1.2.2.1.C.

D. Rise and Fall Time—Same as C.3.1.6.2.2.2.D.

C.3.1.7.2.3 RDAU Connector Signal List

Signal and power connections with the RDAU shall be made through connectors as shown in Table C-8. Pin functions shall be as shown in Table C-9.

C.3.1.7.3 RDAU Secondary Performance Characteristics

C.3.1.7.3.1 Prime Power

The RDAU shall operate from standard single phase 115 vac (rms) plus 15 or minus 10 volts, 60 Hz plus or minus 1.5 Hz power. Input power shall be TBD.

Table C-8

CONNECTOR ASSIGNMENT

Designation	Name		Part Number (Typical)
J1	Analog input	Deutsch	38105N24-61SN
J2	Discrete—input	Deutsch	38105N20-41SN
J3	Terminal I/O	Deutsch	38105N12-10SN
J4	Command output	Deutsch	38105N20-41SW
J5	Power	Deutsch	38105N14-4PN

C. 3. 1. 7. 3. 2 Environment

The RDAU shall be designed to operate in a laboratory environment under the following conditions:

A. Ambient Temperature—10°C to 50°C.

B. Barometric Pressure—Sea level to 5, 000 ft.

C. Relative Humidity—10 to 80 percent.

C. 3. 1. 7. 3. 3 Mechanical

The RDAU shall be designed and constructed consistent with Space Station packaging concepts. No special cooling shall be required.

C. 3. 1. 7. 3. 4 Isolation

Isolation between signal and chassis ground shall be a minimum of 1 megohms at 28 vdc.

Table C-9 (page 1 of 4)
RDAU CONNECTOR AND SIGNAL LIST

Connector	Signal Name	Pin Number	Connector	Signal Name	Pin Number
J1	Analog 1 Hi	A	J1 (Continued)	Analog 11 Hi	X
	Analog 1 Lo	B		Analog 11 Lo	Y
	Analog 1 Shield	-		Analog 11 Shield	-
	Analog 2 Hi	C		Analog 12 Hi	Z
	Analog 2 Lo	D		Analog 12 Lo	a
	Analog 2 Shield	-		Analog 12 Shield	-
	Analog 3 Hi	E		Analog 13 Hi	b
	Analog 3 Lo	F		Analog 13 Lo	c
	Analog 3 Shield	-		Analog 13 Shield	-
	Analog 4 Hi	G		Analog 14 Hi	d
	Analog 4 Lo	H		Analog 14 Lo	e
	Analog 4 Shield	-		Analog 14 Shield	-
	Analog 5 Hi	J		Analog 15 Hi	f
	Analog 5 Lo	K		Analog 15 Lo	g
	Analog 5 Shield	-		Analog 15 Shield	-
	Analog 6 Hi	L		Analog 16 Hi	h
	Analog 6 Lo	M		Analog 16 Lo	i
	Analog 6 Shield	-		Analog 16 Shield	-
	Analog 7 Hi	N		Analog 17 Hi	j
	Analog 7 Lo	P		Analog 17 Lo	k
	Analog 7 Shield	-		Analog 17 Shield	-
	Analog 8 Hi	R		Analog 18 Hi	m
	Analog 8 Lo	S		Analog 18 Lo	n
	Analog 8 Shield	-		Analog 18 Shield	-
	Analog 9 Hi	T		Analog 19 Hi	p
	Analog 9 Lo	U		Analog 19 Lo	q
	Analog 9 Shield	-		Analog 19 Shield	-
	Analog 10 Hi	V		Analog 20 Hi	r
	Analog 10 Lo	W		Analog 20 Lo	s
	Analog 10 Shield	-		Analog 20 Shield	-

Table C-9 (page 2 of 4)

RDAU CONNECTOR AND SIGNAL LIST

Con-nector	Signal Name	Pin Num-ber	Con-nector	Signal Name	Pin Num-ber
J1 (Con-tinued)	Analog 21 Hi	t	J2	Discrete 1 Hi	s
	Analog 21 Lo	u		Discrete 1 Lo	r
	Analog 21 Shield	--		Discrete 1 Shield	-
	Analog 22 Hi	v		Discrete 2 Hi	q
	Analog 22 Lo	w		Discrete 2 Lo	p
	Analog 22 Shield	--		Discrete 2 Shield	-
	Analog 23 Hi	x		Discrete 3 Hi	n
	Analog 23 Lo	y		Discrete 3 Lo	m
	Analog 23 Shield	--		Discrete 3 Shield	-
	Analog 24 Hi	z		Discrete 4 Hi	j
	Analog 24 Lo	AA		Discrete 4 Lo	k
	Analog 24 Shield	--		Discrete 4 Shield	-
	Analog 25 Hi	BB		Discrete 5 Hi	i
	Analog 25 Lo	CC		Discrete 5 Lo	h
	Analog 25 Shield	--		Discrete 5 Shield	-
	Analog 26 Hi	DD		Discrete 6 Hi	f
	Analog 26 Lo	EE		Discrete 6 Lo	g
	Analog 26 Shield	--		Discrete 6 Shield	-
	Analog 27 Hi	FF		Discrete 7 Hi	d
	Analog 27 Lo	GG		Discrete 7 Lo	e
	Analog 27 Shield	--		Discrete 7 Shield	-
	Analog 28 Hi	HH		Discrete 8 Hi	c
	Analog 28 Lo	JJ		Discrete 8 Lo	b
	Analog 28 Shield	--		Discrete 8 Shield	-
	Analog 29 Hi	KK		Discrete 9 Hi	a
	Analog 29 Lo	LL		Discrete 9 Lo	z
	Analog 29 Shield	--		Discrete 9 Shield	-
	Analog 30 Hi	MM		Discrete 10 Hi	y
	Analog 30 Lo	NN		Discrete 10 Lo	x
	Analog 30 Shield	PP		Discrete 10 Shield	-

Table C-9 (page 3 of 4)
RDAU CONNECTOR AND SIGNAL LIST

Connector	Signal Name	Pin Number	Connector	Signal Name	Pin Number
J2 (Continued)	Discrete 11 Hi	A	J4 (Continued)	Command 4 Lo	k
	Discrete 11 Lo	B		Command 4 Shield	-
	Discrete 11 Shield	-		Command 5 Hi	i
	Discrete 12 Hi	C		Command 5 Lo	h
	Discrete 12 Lo	D		Command 5 Shield	-
	Discrete 12 Shield	-		Command 6 Hi	f
	Discrete 13 Hi	E		Command 6 Lo	g
	Discrete 13 Lo	F		Command 6 Shield	-
	Discrete 13 Shield	-		Command 7 Hi	d
	Discrete 14 Hi	G		Command 7 Lo	e
	Discrete 14 Lo	H		Command 7 Shield	-
	Discrete 14 Shield	-		Command 8 Hi	c
	Discrete 15 Hi	J		Command 8 Lo	b
	Discrete 15 Lo	K		Command 8 Shield	a
	Discrete 15 Shield	-		Command 9 Hi	z
	Discrete 16 Hi	L		Command 9 Lo	-
	Discrete 16 Lo	M		Command 9 Shield	y
	Discrete 16 Shield	N		Command 10 Hi	x
				Command 10 Lo	-
J4	Command 1 Hi	s		Command 10 Shield	A
	Command 1 Lo	r		Command 11 Hi	B
	Command 1 Shield	-		Command 11 Lo	-
	Command 2 Hi	q		Command 11 Shield	C
	Command 2 Lo	p		Command 12 Hi	D
	Command 2 Shield	-		Command 12 Lo	-
	Command 3 Hi	n		Command 12 Shield	E
	Command 3 Lo	m		Command 13 Hi	F
	Command 3 Shield	-		Command 13 Lo	-
	Command 4 Hi	j		Command 13 Shield	G

Table C-9 (page 4 of 4)

RDAU CONNECTOR AND SIGNAL LIST

Connector	Signal Name	Pin Number	Connector	Signal Name	Pin Number
J4 (Continued)	Command 14 Hi	H	J3 (Continued)	Data Input Hi	G
	Command 14 Lo	-		Data Input Lo	K
	Command 14 Shield	J		Data Shield	J
	Command 15 Hi	K		Data Output Hi	F
	Command 15 Lo	-		Data Output Lo	E
	Command 15 Shield	L		Data Shield	D
	Command 16 Hi	M		Spare	C
	Command 16 Lo	N			
	Command 16 Shield		J5	115V, 60 Hz Power	A
				115V, 60 Hz Power	B
J3	Clock Hi	H		Ground	C
	Clock Lo	A		Spare	D
	Clock Shield	B			

Appendix D

DISPLAY INTERFACE ADAPTER SPECIFICATION

IMS-DIA-001

D.1 SCOPE

This specification establishes requirements for design, performance, fabrication, and acceptance of the display and control (D&C) interface adapter to be incorporated into the IMS special emphasis task, displays and controls breadboard.

D.1.1 Purpose

The D&C interface adapter (DIA) provides an operational interface between the data bus terminal and the D&C console equipment. This adapter shall accept serial input display data and clock signals from the data bus terminal, provide required decode conversion, buffering, and storage of these signals, and provide data output signals driving the display and control equipments.

D.2 APPLICABLE DOCUMENTS

A. Exhibit "C", Space Station Phase "B" Extension, Statement of Work for IBM, Inc., 2 February 1971

B. Subcontract MDAC WD-69-1-017, Exhibit "B" Statement of Work, Space Station Phase "B" Extension 18 November 1970.

D.3 REQUIREMENTS

The DIA shall provide interface and data transfer media between the data bus terminal and the display and control equipment as illustrated in Figure D-1. It shall accept input data and commands, provide decoding and display destination selection, supply required buffering, and provide output signal interfaces for the individual display units. The DIA shall accept and transfer control commands from console switches and input devices to the data bus terminal (DBT).

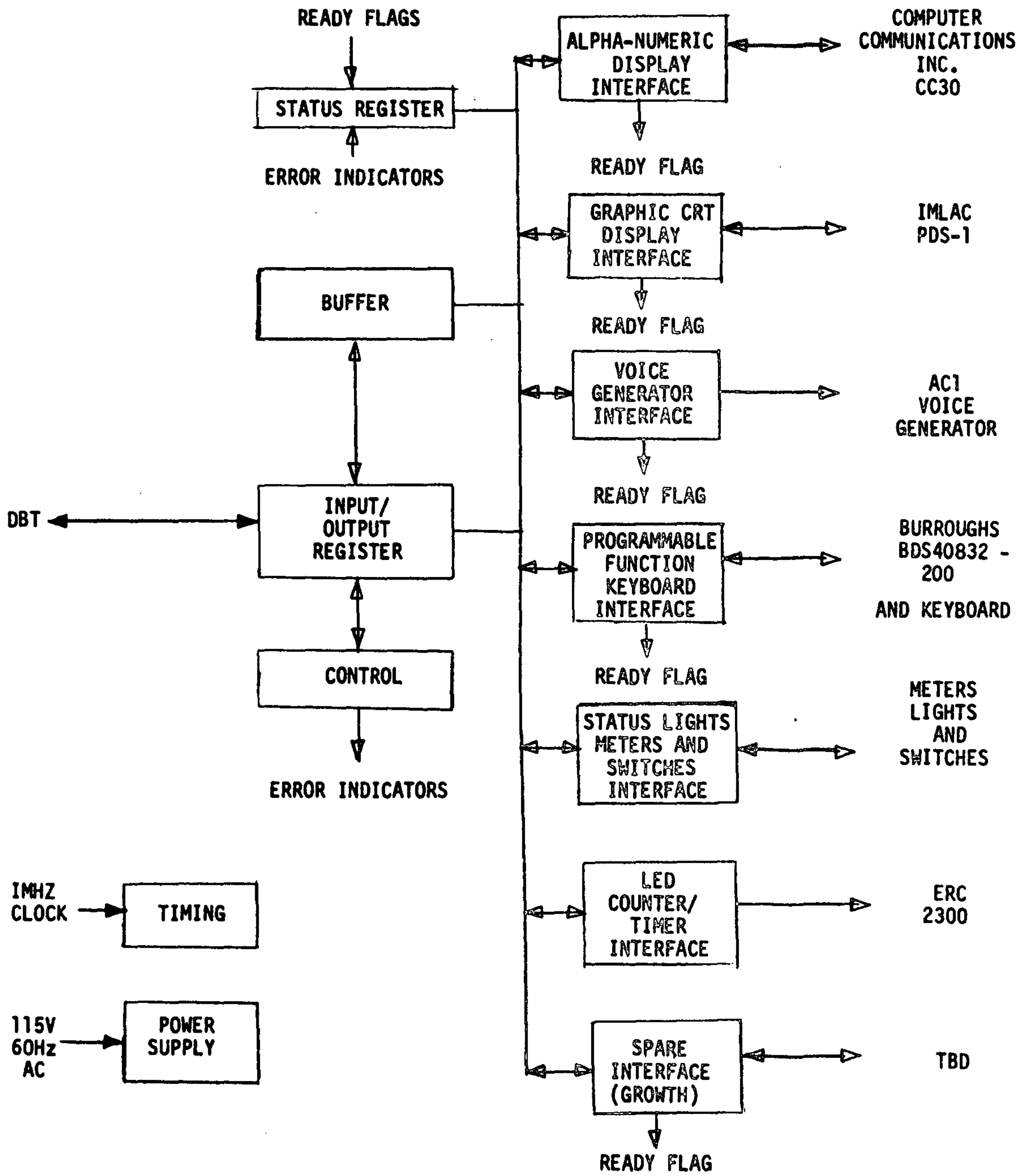


Figure D-1. Display Interface Adapter Block Diagram

D.3.1 Function

The DIA shall communicate with a DBT via a 1 MHz serial I/O channel and with control and display devices over special interfaces. The control and display devices shall include a graphic CRT display, an alphenumeric display, a programmable function keyboard and display, a voice response unit, miscellaneous status lights, meters, and switches; and a spare (growth) interface. Figure D-1 provides a block diagram of the primary logic functions. Included is an input/output register for transferring data in and out of the unit, control logic for decoding instructions and directing operations, a buffer for temporary data storage, a status register to permit interrogation of detected errors/ready flags, and seven interface logic groups for communication with the indicated display equipment.

D.3.1.1 Data Bus Terminal Interface

The DIA shall be capable of receiving serial instructions and data from a DBT along with a 1 MHz clock, and of transmitting serial data to a DBT using the received clock. The received clock shall be used by the DIA for timing and message synchronization and shall provide the basis for internal logic operation. Data formats and the operations to be performed are described in the following sections.

D.3.1.1.1 Control

The DIA shall contain logic for decoding and performing control functions as specified by the received instruction words. A flow diagram is provided in Figure D-2 to indicate the sequence of operation. All functions requiring a response to the DBT shall initiate a data transfer within the time period not to exceed 100 microseconds.

D.3.1.1.2 Error Detection

The DIA shall check all incoming messages for odd parity. In the event a parity is detected, the operation shall stop and the DIA logic shall return to the initial state for that message unless otherwise specified herein. In any case, the parity error flag in the status word (D.3.1.1.3.3) will be set to logic "1."

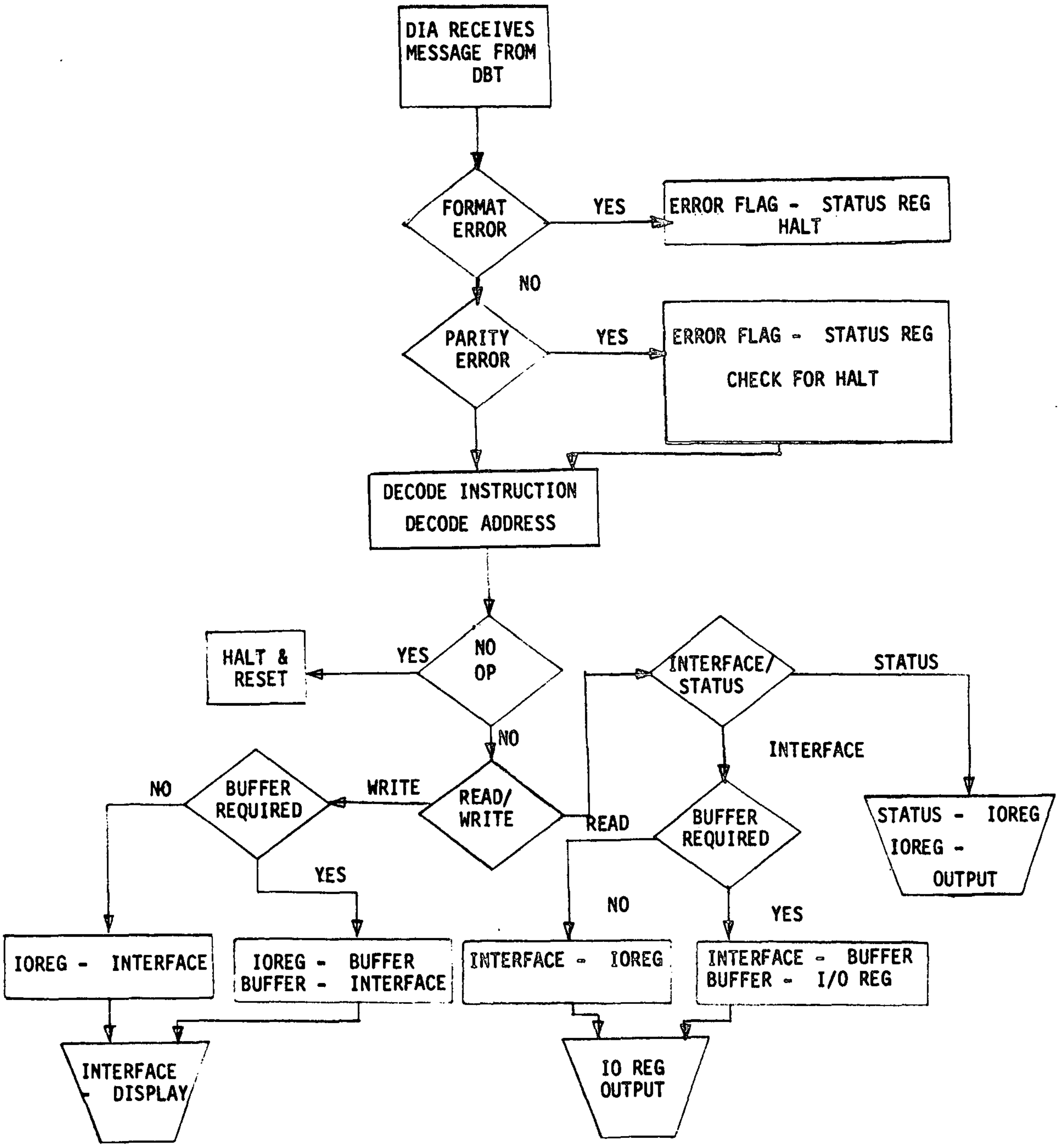


Figure D-2. DIA Functional Flow

In the event that an invalid address or operation code or other format error is detected, the message will be rejected and the format error flag in the status word will be set to logic "1."

In the event of improper response from any display or control interface, the system error flag in the status word shall be set to logic "1," and the logic shall return to the initial state for that message.

D. 3. 1. 1. 3 <u>Format</u>

Each action by the DIA shall be initiated by a command word. Command words may be followed by data words. When a response is required, data words shall comprise the response.

D. 3. 1. 1. 3. 1 Command Format

The format for command words output by the DBT shall be as shown below. The most significant bit shall be transmitted first. Command message synchronization shall be accomplished by detection of a missing pulse in the DBT clock signal as defined in the IMS breadboard data bus specification, C. 3. 1. 6. 1. 6. 1.

Command Format:

MSB LSB

L	1	2	3 4 5 6 7	8 9 10 11	12 13 14	15 16	
1	0	1	Count Field	Instruction	Address	Spare	P

Constant

L = Lead one

P = Parity, odd

LSB = Least-significant bit

MSB = Most-significant bit

D. 3. 1. 1. 3. 1. 1 Word Count Field

Bit 3 to 7 shall define the binary number of 18-bit data words (16 bits of data content) to follow the command word. It defines the number of words being read into the DIA or the number of words being read out. The maximum number possible is 32 words. Binary zero (00000) in the count field shall denote 32 words. All other word counts shall be represented directly by their binary equivalent.

D. 3. 1. 1. 3. 1. 2 Instruction Field

Bits 8 through 11 comprise the instruction field. Instructions initiate the action required of the DIA and are described in Table D-1.

D. 3. 1. 1. 3. 1. 3 Address Field

Bits 12 through 15 comprise the address field and select the interface group which will be affected. Address field definition is as shown in Table D-2.

D. 3. 1. 1. 3. 2 Data Format

Data immediately follows a write instruction to the DIA, and comprises the DIA's response on read instructions. For data from the DBT to the DIA, the format is as follows:

MSB LSB

L	1 2 ----------------------------------	16
0	Data Field	P

Table D-1

INSTRUCTION FIELD

Bits 8	9	10	11*	Instruction Name	DIA Reaction
0	0	-	-	No operation	Causes DIA to cease operation in process and reset to initial state.
1	1	-	-	Write	Causes data in succeeding words to be transferred to a display interface.
0	1	-	-	Read	Causes data to be requested from a display interface.
1	0	-	-	Command	Causes one of four commands or discrete actions to be performed as selected by bits positions 10 and 11.

*Bits 10 and 11 may be used as modifier bits and/or may be used for expansion except as noted in case of a command instruction.

Table D-2

ADDRESS FIELD

Bits	12	13	14	15	
	0	0	0	0	Not used
	0	0	0	1	Graphic display
	0	0	1	0	Alpha numeric display
	0	0	1	1	Voice generator
	0	1	0	0	Programmable function display
	0	1	0	1	Switches, lights and status register (includes switches and lights associated with programmable function keyboard)
	0	1	1	0	LED event timer
	0	1	1	1	LED calendar clock
	1	0	0	0	Meters*
	1	0	0	1	Growth interface

*The meter selection and meter voltage level shall be contained in the data words that follow this command.

Transmission of data from the IDA to the DBT shall be in the same format, except that the lead bit shall be "1" instead of "0."

D. 3. 1. 1. 3. 3 Status Format

The DIA shall contain a status register that permits monitoring of detected errors and interface operating status bits. Readout of the status register shall be in the general format of a data word with bits positions defined as follows:

A. Parity Error—When a parity error is detected, this bit shall be set, operation shall stop, and the DIA logic shall return to the initial state for that message. The bit shall be reset following executive of a read status command from the DBT.

B. Format Error—When an invalid address or operation code or other format error is detected, the bit shall be set, and the message shall be rejected. The bit shall be reset following execution of a read status command from the DBT.

C. System Error—This bit shall be set upon detection of improper response from a display or control interface, and shall be reset following execution of a read status command from the DBT.

D. Alphanumeric Transmit Request—This bit shall be set upon receipt of the transmit request signal from the CC-30 video CRT display and shall be reset when the transmit request signal is dropped (D. 3. 1. 2. 2. 2. 2).

E. Alphanumeric Reject to Computer—This bit shall be set upon receipt of the reject to computer or master clear signal from the alphanumeric unit during an alphanumeric read or write operation, and shall be reset following execution of a read status command from the DBT. (D. 3. 1. 2. 2. 1. 5 and D. 3. 1. 2. 2. 1. 8.)

F. Graphic Display Transmit Request—This bit shall be set upon receipt of a transmit request from the PDS-1 graphic display. It shall be reset following execution of a read graphic display command from the DBT (D. 3. 1. 2. 1. 3. 2).

G. Voice Terminal Ready—This bit shall be set when the VTE message storage section is ready to receive a new word or series of words and shall be reset upon receipt of a write voice generator command from the DBT (D. 3. 1. 2. 3. 5).

H. Growth Interface Ready—This bit is reserved for future capability and will be defined at a later time.

D. 3. 1. 1. 4 <u>DIA to DBT Interface Characteristics</u>

The interface between the DIA and the DBT shall meet the requirements of the IMS breadboard data bus specification, C. 3. 1. 6. 1. 6. Data inputs/outputs with the DBT shall be by connector J9 (DBT interface) and shall be a Deutsch Part Number 38105 N12-10SN.

D. 3. 1. 2 Display Console Equipment Interface

The DIA shall provide outputs to the console equipment upon receipt of display destination addressing signals and data from the data bus terminal equipment.

D. 3. 1. 2. 1 Multifunctional CRT Display

The DIA shall output to a multifunctional CRT display terminal, upon proper addressing decoding, the data received from the data bus terminal. These data are converted into alphanumeric characters and symbols, graphical figures, and other types of computer-generated information for display presentation. The DIA shall also receive data from the display for transmission to the data bus terminal. The display device will be a PDS-1 programmable display system, manufactured by IMLAC Corporation. The PDS-1 display will contain a CRT display screen, a solid state alphanumeric/function keyboard, and interactive light pen, and will operate from a self-contained display processor and minicomputer.

D. 3. 1. 2. 1. 1 PDS-1 Description

The PDS-1 employs a digital display processor to execute character subroutines. These subroutines generate digital codes which control CRT beam movements by means of D/A converters. All alphanumeric and graphic symbols generated are displayed as a connected string of vector strokes. All such strokes are coded in eight-bit bytes (two per memory word) which are stored in core as character subroutines. The system can display about 1, 200 characters or 300/900 in. of graphics or combination of characters and graphics, depending on the efficiency of the symbol definitions in the program. The display screen of the terminal is a 14-in. CRT refreshed from local core memory at 40 frames per second. The CRT can display 128 characters per line by 40 lines. The resolution of the display system is analog adjustable, up to 1, 024 points in X and 1, 024 points in Y.

In addition to the display processor, a general purpose minicomputer sharing the same core memory is incorporated to generate subroutine call lists in core that the display processor then executes.

The keyboard is divided into two sections: one is similar to a standard teletype keyboard, and the second is a set of special function keys used for editing, transmission control, and cursor movement.

A lightpen is available for specific graphics or text interactive modes of operation where the keyboard is inappropriate for the desired human response times. The DIA shall provide the following interfaces with the multifunctional CRT display.

D. 3. 1. 2. 1. 2 Display Inputs

Transfer of data between the DIA and the display shall be by 16-bit parallel words in conjunction with input/output control signals. This interface shall be via the PDS-1 IEI-1 I/O expansion and external interrupt interface option. Signal characteristics for these interface lines are shown below and are typical for 7400-series logic manufactured by Texas Instruments, as described in TI Catalog CC201.

	Minimum	Typical	Maximum
Low-level output voltage		0. 22	0. 40 volts
High-level output voltage	2. 4	3. 3	volts
Low-level output sink capability:			
gates			16. 0 mA
buffers			48. 0 mA
High-level output source capability:			
gates			400 A
buffers			1. 2 mA
Output reverse current			250 A
Input low-level current			-1. 6 mA
Input high-level current			40 A

Signal inputs to the PDS-1 shall be provided by open collector 7400 series "nand" gates or equivalent. The collector resistor is 330 to +5 vdc and is supplied by the PDS-1. Up to twenty gates may be connected to a single input in wired "or" configuration.

D. 3. 1. 2. 1. 3 Data Transfer

Transfer of data to and from the display is in the form of 16-bit parallel characters. All input and output data transfers take place under PDS-1 program control via a 16-bit accumulator. The accumulator input and output functions use the same interface pins, and negative logic is employed. Transfer of data words is a maximum rate of 60×10^3 words per second where status-checking is required, and 100×10^3 words per second without status-checking.

D. 3. 1. 2. 1. 3. 1 I/O Operation

I/O operations are controlled by the PDS-1 using the instruction 001ABP, where AB selects the desired external device and P selects one of three timing pulses to be used by the device for transfer control. The A and B characters are each represented by three bits of code. These are decoded internally and presented at the I/O connector as six lines for a (I0A2 through IA07) and eight lines for B (I0B0 through I0B7). Positive logic is used. (The remaining two A lines are reserved for internal use.) Capability is thus provided for addressing up to 48 external devices or functions. Three timing pulses (P1, P2, P3) controlled by the three-bit character P are also available at the I/O connector. Interface control signals generated by the DIA include data in and out lines, an external interrupt, and an external skip line. Instruction format and timing diagrams are shown in Figure D-3.

I/O Instruction Format

MSB LSB

0	1 2 3	4 5 6	7 8 9	10 11 12	13 14 15
0	0	1	A Device	B Number	P P3 P2 P1

D. 3. 1. 2. 1. 3. 2 Data Output from PDS-1

Data output operations will be initiated under PDS-1 program control by output of a status-check instruction. This instruction will raise the I0A7 and I0B2 device selection lines and the P3 timing pulse. The DIA shall recognize this combination of interface signals as an indication that data are available for output, and will set the graphic display ready bit in the status word and wait for a read graphic display command from the data bus. Upon receipt of this command, the DIA shall generate an interrupt signal to

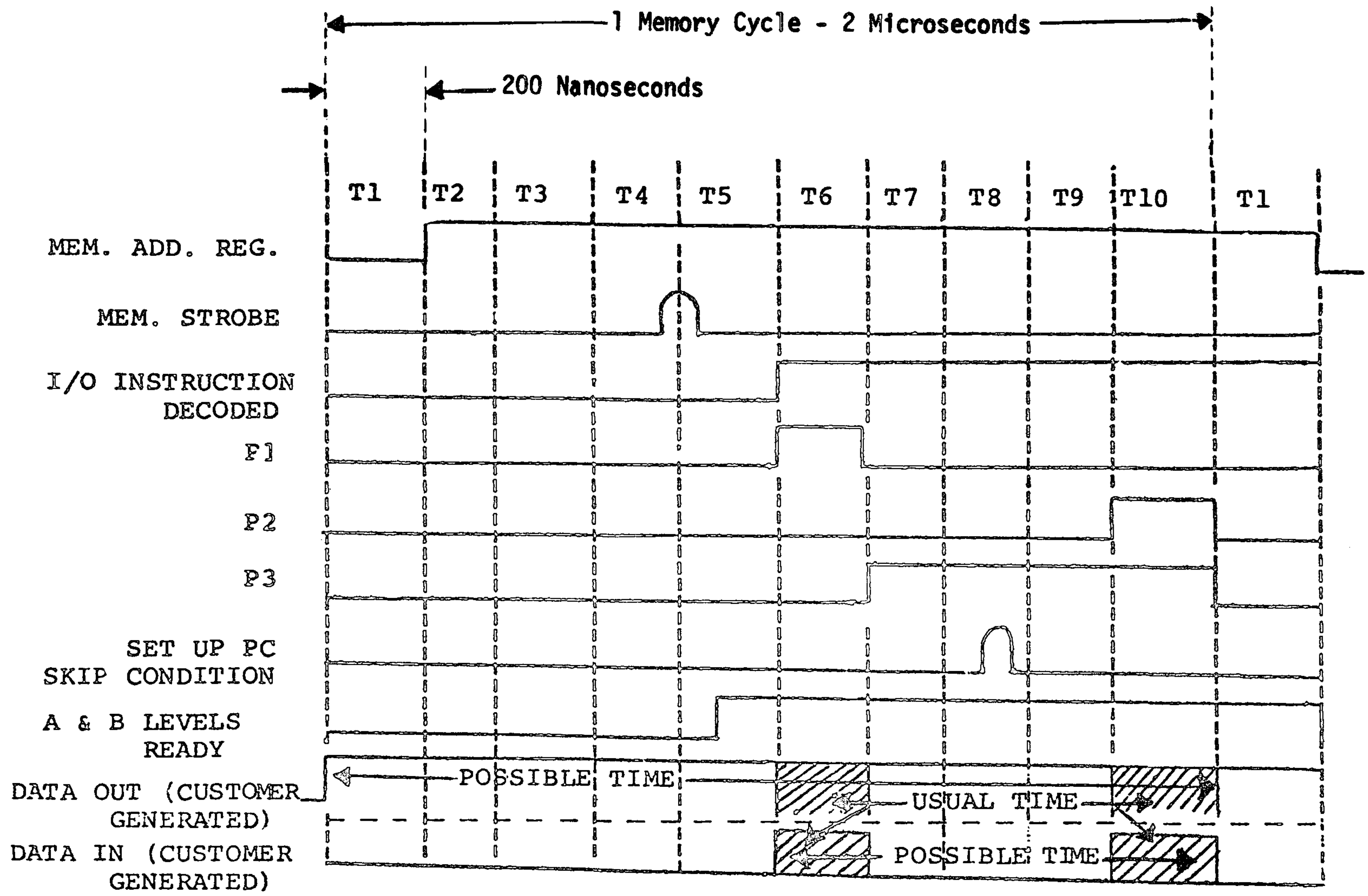


Figure D-3. PDS-1 I/O Timing

the PDS-1 by switching the External Interrupt interface line to logic "0." The PDS-1 will then verify the source of the interrupt by executing an "interrupt status read" instruction as described in D. 3. 1. 2. 1. 3. 4, and will execute the data output subroutine. This subroutine will begin with the status-check instruction (I0A7, I0B2, P3) described above. The first execution of this subroutine instruction will occur not later than 40 μsec after the interrupt and will be repeated at intervals of 4 μsec until the DIA indicates that it is ready to accept the data word. When ready to accept the first data word, the DIA shall notify the PDS-1 by switching the External Skip interface line to logic "0" during the P3 interval of the status-check instruction. The PDS-1 will then execute a data output instruction. This instruction will raise the I0A7 and I0B2 device selection lines and the P1 and P2 timing pulses. The DIA shall take the parallel data during the P1 or P2 interval and during the same interval shall switch the Data Out line to logic "0." Subsequent data words in each block transfer will be output in the same manner, except that no interrupt shall be generated. Each data output instruction will be preceded by one or more status check instructions, and data will be transferred following receipt of the External Skip signal indicating that the DIA is ready to receive. The minimum time interval between the completion of a data output instruction and beginning of the subsequent status check instruction by the PDS-1 will nominally be 12μsec, and the status check instruction will be repeated at 4-μsec intervals until the External Skip is received. All output data transfers will occur in blocks of 32 16-bit words.

D. 3. 1. 2. 1. 3. 3 Data Input to PDS-1

When a write graphic display command is received from the data bus, the DIA shall switch the External Interrupt interface line to logic "0." The PDS-1 will then verify the source of the interrupt by executing an interrupt status read instruction as described in D. 3. 1. 2. 1. 3. 4 and will execute the data input subroutine. This subroutine will begin with a status-check instruction. This instruction will raise the I0A7 and I0B1 device selection lines and the P3 timing pulse. The first execution of this instruction will occur not later than 40 μsec after the interrupt and will be repeated at 4-μsec intervals until a ready indication is received. When ready to transfer the first word, the DIA shall so indicate by switching the $\overline{\text{External Skip}}$ interface line to logic "0" during the P3 interval of the status check instruction. The PDS-1 will then execute a data input instruction. This instruction will raise the IOA7 and IOB1 device selection lines and the P1 and P2 timing pulses. The DIA shall gate the parallel data lines to the PDS-1 during the P1 or P2 interval, and during the same interval shall switch the $\overline{\text{Data In}}$ interface line to logic "0." Subsequent data words in each block transfer will be transferred in the same manner, except that no interrupt will be generated. Each data input instruction will be preceded by the status check instruction to verify that data are ready. The time interval between words will be the same as that described in the previous section for data outputs. The block length of data inputs will be specified as described in D. 3. 1. 2. 1. 3. 4.

D. 3. 1. 2. 1. 3. 4 Interrupt Status and Input Word Count

The DIA shall be capable of generating an interrupt signal to the PDS-1 during data output and input operations as described in the previous sections. This shall be done by switching the $\overline{\text{External Interrupt}}$ line to logic "0." Upon receipt of the interrupt signal, the PDS-1 will generate an interrupt status read instruction to determine the source of the interrupt. This instruction will raise the IOA7 and IOB0 device selection lines and the P1 and P2 timing pulses. The DIA shall indicate the interrupt source by switching the appropriate parallel data interface line to logic "0" during the P1 or P2 interval, and during the same interval shall switch the $\overline{\text{Data In}}$ line to logic "0." A data input (to the PDS-1) interrupt shall be indicated on the $\overline{EI_0}$ line, and a data output interrupt on the $\overline{EI_1}$ line. All other lines shall be a logic level "1" during this instruction, except that in the case of a data input interrupt, bits four through eight (EI_4 - EI_8) shall contain the word count as specified in the read command.

D. 3. 1. 2. 1. 3. 5 Start Clear Signal

The Start Clear signal on the I/O connector produces a positive-going pulse whenever the PDS-1 is started. This signal is provided to use in initializing external I/O controllers if required.

D. 3. 1. 2. 1. 3. 6 Parity Error

In the event that a parity error is detected in the data being loaded into the PDS-1, the loading operation shall be completed and the Parity Error bit in the status word shall be set.

D. 3. 1. 2. 1. 4 Connectors/Pin Assignments

Interface connectors and pin assignments shall be as defined in Table D-3. All interfacing wiring shall be twisted pairs.

D. 3. 1. 2. 2 Video CRT Display

The DIA shall interface with a Computer Communications, Inc., Model CC-30 video CRT display. This device has the capability of displaying alphanumeric and limited graphic information on a standard 525-line television monitor. Data are input via the DIA from the data bus. The device includes a alpha-numeric keyboard to allow an operator to enter data for transmission via the data bus. An internal 1,024-character random-access core memory provides display refresh and keyboard buffering.

Data inputs to the CC-30 are received from the DBT in the form of 16-bit words, each containing two characters. The word format is shown below:

<table>
<tr><td>L</td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td><td>9</td><td>10</td><td>11</td><td>12</td><td>13</td><td>14</td><td>15</td><td>16</td></tr>
<tr><td>0</td><td colspan="7">A</td><td>Fa</td><td colspan="7">B</td><td>Fb</td><td>P</td></tr>
</table>

A and B are each a 7-bit character codes. Fa and Fb denote whether the character codes represent data or function codes (F = 0 denotes data, F = 1 denotes function).

D. 3. 1. 2. 2. 1 Input/Output Channel Operation

A. Computer Input Channel—The computer input channel is a high-speed parallel channel consisting of the following signals:

8 data signals

4 control signals

1 timing signal

Table D-3

J1 - PDS-1 INPUT/OUTPUT INTERFACE

Deutsch P/N 450-24-61P

Pin	Function	Pin	Function	Pin	Function
A	Not Used	Y	$\overline{EI}_9$	u	$\overline{\text{Data Out}}$
B	Not Used	Z	Common	v	Common
C	Not Used	a	$\overline{EI}_{10}$	w	I0A7
D	$\overline{EI}_0$	b	Common	x	Common
E	Common	c	$\overline{EI}_{11}$	y	I0B0
F	$\overline{EI}_1$	d	Common	z	Common
G	Common	e	$\overline{EI}_{12}$	AA	I0B1
H	$\overline{EI}_2$	f	Common	BB	Common
J	Common	g	$\overline{EI}_{13}$	CC	I0B2
K	$\overline{EI}_3$	h	Common	DD	Common
L	Common	i	$\overline{EI}_{14}$	EE	I0B7
M	$\overline{EI}_4$	j	Common	FF	Common
N	Common	k	$\overline{EI}_{15}$	GG	I0P1
P	$\overline{EI}_5$	m	Common	HH	Common
R	Common	n	$\overline{\text{Ext. Int.}}$	JJ	I0P2
S	$\overline{EI}_6$	p	Common	KK	Common
T	Common	q	$\overline{\text{Ext Skip}}$	LL	I0P3
U	$\overline{EI}_7$	r	Common	MM	Common
V	Common	s	$\overline{\text{Data In}}$	NN	Start Clear
W	$\overline{EI}_8$	t	Common	PP	Common
X	Common				

All data transmission from the CC-301 Controller to the DIA occur on this channel. The operation is initiated when the CC-301 informs the DIA via a Transmit Request line that it has one or more data words ready for transmission. The DIA responds with an Input Request signal when it is ready to accept the data. The CC-301 informs the DIA by an Input Resume (data strobe) control line that it has placed a word on the data lines. The DIA will then drop the Input Request line. After the CC-301 transmits the last data word, it will drop the Transmit Request line. In addition to these various control and data communications lines, there is a fourth control line designated Master Clear and a line to carry a timing signal to the DIA. The Master Clear line, when raised, indicates the Master Clear switch in the CC-301 is being depressed. The timing signal, which is derived from the CC-301 main clock, synchronizes the appropriate channel adapter and the CC-301 Controller.

B. Computer Output Channel—The computer output channel is a high-speed channel consisting of the following signals:

   8 data signals
   5 control signals
   1 clock signal

Data transfers from the DIA to the CC-301 Controller are initiated by the DIA. The DIA raises its Output Request line when it has data ready for transmission. If a parity error is present in the data word, the Parity Error line should also be raised with the Output Request line. If the DIA is not selected for input to the CC-301, a Reject line is raised by the CC-301. If the DIA is selected for input to the CC-301 Controller, an Output Resume (data strobe) line is raised by the CC-301. This strobe signal transfers the DIA output data lines into the CC-301 I/O Data Register. If the next output data word is not immediately available, the Output Request line should be dropped. Should the data word be a function command, a Function Request line rather than the Output Request line is raised by the DIA. Again, as in the Computer input channel, there is a Clock line.

D. 3. 1. 2. 2. 1. 1 Data Input

The DIA shall input data to the CC-30 in the form of 7-bit parallel characters, plus even parity. Data transfers are controlled by a clock signal from the CC-30 and by a series of control signals as defined below. Maximum data rate shall not exceed 500, 000 characters per second. As the data word received from the DBT will not contain a parity bit for this input, the parity bit must be generated by the DIA. The parity bits replace the function bits Fa and Fb, which are not transferred to the CC-30.

D. 3. 1. 2. 2. 1. 2 Clock

The input clock signal (T-11-750) from the CC-30 is a positive pulse of approximately 100 nanoseconds duration and 920 nanoseconds period. Rise and fall times are approximately 30 nanoseconds.

D. 3. 1. 2. 2. 1. 3 Output Request

The Output Request line shall be raised by the DIA to notify the CC-30 that data are available. This signal shall be raised in sync with the leading edge of the input clock. The signal shall be held high until the leading edge of the first clock pulse following Output Resume (D. 3. 1. 2. 2. 1. 5).

D. 3. 1. 2. 2. 1. 4 Parity Error

If the character to be transferred to the CC-30 contains a detected parity error, the DIA shall raise the Parity Error signal at the same time as the Output Request. The CC-30 will accept the character but will display a special parity error symbol at that character position on the screen. The Parity Error signal shall be dropped at the leading edge of the first clock following Output Resume (D. 3. 1. 2. 2. 1. 6).

D. 3. 1. 2. 2. 1. 5 Reject to Computer

If the CC-30 has not been properly set up to accept computer data, a Reject to Computer signal will be generated. This will be a 100-nanosecond pulse occuring 0. 5 + N microseconds following the leading edge of the Output Request. N may vary from 0 to 40 microseconds. This line shall be terminated with a load of 510 ohms to +5 VDC, or the current equivalent. The DIA shall store the reject to computer signal in the status register and I/O operation shall cease.

D. 3. 1. 2. 2. 1. 6 Output Resume

If the CC-30 is ready to accept data, it will generate an Output Resume signal. This will be a 100-nanosecond pulse occuring 0. 5 + N microseconds after the leading edge of Output Request. N will vary from 0 to 40 microseconds. The DIA shall use the Output Resume signal to gate the seven data bits and the parity bit to the CC-30.

D. 3. 1. 2. 2. 1. 7 Function Request

The Function Request signal shall be used in the same manner as the Output Request when a function command rather than data is being transferred to the CC-30.

D. 3. 1. 2. 2. 1. 8 Master Clear

A Master Clear line is used by the CC-30 to indicate to the DIA when a master clear operation is in progress. (This operation may be initiated via the data bus or by keyboard command.) The line is at logic "0" for the duration of the Master Clear operation. If this occurs during an input or output operation, the Master Clear signal shall be stored in the status register as a "reject to computer" function and the I/O operation will be terminated.

D. 3. 1. 2. 2. 2 Data Output

The DIA shall accept data from the CC-30 in the form of 7-bit parallel words plus even parity. Data transfers shall be controlled by a clock signal and a series of control signals as defined below.

D. 3. 1. 2. 2. 2. 1 Clock

The output clock signal (T-11-275) from the CC-30 is a positive pulse of approximately 100 nanoseconds duration and 920 nanoseconds period. Rise and fall times are approximately 30 nanoseconds.

D. 3. 1. 2. 2. 2. 2 Transmit Request

The CC-30 raises the Transmit Request line to indicate to the DIA that data are available. The DIA shall set the Alphanumeric Transmit Request bit in the status word and wait for an alphanumeric Read command from the data bus.

D. 3. 1. 2. 2. 2. 3 Input Request

When the DIA is ready to accept data, it shall raise the Input Request signal in sync with the leading edge of the CC-30 clock. The signal shall be dropped at the leading edge of the first clock following Input Resume.

D. 3. 1. 2. 2. 2. 4 Input Resume

The CC-30 will respond to the Input Request with an Input Resume signal. This signal will occur approximately 0. 5 + N microseconds after the leading edge of Input Request. N may be 0 to 40 microseconds. The Input Resume signal is a 100-nanosecond pulse and shall be used by the DIA to strobe the data lines from the CC-30. The data lines are stable until approximately 100 nanoseconds after the trailing edge of Input Resume.

D. 3. 1. 2. 2. 3 Interface Signal Characteristics

The CC-30 utilizes Signetics series 600 DTL logic elements. Nominal logic levels are +0. 5 volt for logic 0 and +4. 5 volts for logic 1. Interface signals shall be referenced to a signal return connection from the CC-30.

D. 3. 1. 2. 2. 4 Connector/Pin Assignment

The interface connector on the DIA shall be as defined in Tables D-4 and D-5.

Note: The Transmit Request line will be held high until all available data have been output from the CC-30. If greater than 32 16-bit words, the DIA shall reset the Alphanumeric Transmit Request status bit after the 32nd word and wait for another read command from the data bus. If the number is less than the number specified in the command word count field the missing word spaces shall be filled with zeros by the DIA.

Table D-4

J2 CC-30 DATA INPUT—DEUTSCH PART NUMBER 450-14-19-PN

Pin	Function
A	Not used
B	Not used
C	Not used
D	Not used
E	$\overline{\mathrm{SIODR\ 1B}}$ (LSB)
F	$\overline{\mathrm{SIODR\ 2B}}$
G	$\overline{\mathrm{SIODR\ 3B}}$
H	$\overline{\mathrm{SIODR\ 4B}}$
J	$\overline{\mathrm{SIODR\ 5B}}$
K	$\overline{\mathrm{SIODR\ 6B}}$
L	$\overline{\mathrm{SIODR\ 7B}}$
M	$\overline{\mathrm{SIODR\ 8B}}$ (Parity)
N	Output Request
P	Parity Error in Computer
R	Function Request
S	Output Resume
T	Reject to Computer
U	T-11-750
V	Signal Return

D. 3. 1. 2. 3 Speech Generator

The DIA shall interface with Advanced Communications Corporation Voice Terminal Equipment (VTE). This device is a solid-state voice synthesizer having a digitally stored vocabulary designed to generate clear, distinct voice messages on command. These messages may consist of individual words, or phrases containing several words. Vocabulary selection commands are provided via the data bus in the form of 8-bit digital codes. Details of the interface are described in the following sections.

Table D-5

J3 CC-30 DATA OUTPUT—DEUTSCH PART NUMBER 450-14-19-SN

Pin	Function
A	Not used
B	Not used
C	Not used
D	Not used
E	IODR 1 (LSB)
F	IODR 2
G	IODR 3
H	IODR 4
J	IODR 5
K	IODR 6
L	IODR 7
M	IODR 8 (Parity)
N	Input Request
P	Xmit Request
R	Input Resume
S	Not used
T	T-11-275
U	Master Clear
V	Signal Return

D. 3. 1. 2. 3. 1 Message Selection Code

The DIA shall present Message Selection codes to the VTE in the form of 8-bit parallel words. Upon presentation, these signals shall be held stable until receipt of end of message signal from the VTE. Rise and fall times of the signals shall be less than 10 microseconds.

D. 3. 1. 2. 3. 2 Message Ready Signal

The DIA shall indicate the availability of the message selection code by a Message Ready signal input to the VTE. This signal may begin any time after the Message Selection lines have become stable and shall remain true until receipt of the end of message signal from the VTE.

D. 3. 1. 2. 3. 3 End of Message Signal

The VTE shall indicate completion of message generation by an End of Message signal to the DIA. The duration of this signal shall be 10 ±2 microseconds.

D. 3. 1. 2. 3. 4 Signal Termination Characteristics

The interface lines between the DIA and the VTE shall be single-ended referenced to a common signal ground. Signal ground shall be isolated from chassis ground by a minimum of 10 megohms. Interface signals shall be standard TTL levels to and from 7400 series logic elements.

D. 3. 1. 2. 3. 5 Message Storage

The DIA shall have the capability of accepting and storing message selection codes for up to five spoken words from the DBT while awaiting the VTE to complete individual words being constructed into phrases. Upon completion of each spoken word, the VTE will indicate to the DIA this condition via the end of message signal (Refer to Paragraph D. 3. 1. 2. 3. 3). After a short time delay of TBD milliseconds, the DIA shall output the message selection code for the subsequent word and the message-ready signal.

D. 3. 1. 2. 3. 6 Parity Error

In the event the DIA detects a parity error, no output to the VTE shall result.

D. 3. 1. 2. 3. 7 Connector/Pin Assignments

The interface connector shall be Deutsch Part No. 450-14-15-PN. Pin assignments shall be as shown in Table D-6.

Table D-6

INTERFACE CONNECTOR DEUTSCH PART NUMBER 450-14-15-PN

Pin	J4 Voice Terminal Equipment Function
A	Not used
B	Not used
C	Not used
D	Data Bit 1
E	Data Bit 2
F	Data Bit 3
G	Data Bit 4
H	Data Bit 5
J	Data Bit 6
K	Data Bit 7
L	Data Bit 8 (LSB)
M	Message Ready
N	End of Message
P	Signal Return
R	Not used

D. 3. 1. 2. 4 Programmable Functional Keyboard (PFK)

The DIA shall output data signals to the PFK upon proper address decoding of data received from the data bus terminal. There data will be converted into alphanumeric characters by the PFK. The DIA shall also accept switch contact closure discrete events and provide addressing codes for transfer of this discrete event to the data bus terminal.

D. 3. 1. 2. 4. 1 Display Interface Signals

The readout display requires 6-bit parallel inputs entered into its internal memory and a series of control signals. Data will be entered sequentially; first character - row one, column one, then from left to right, top to bottom until the complete display of 256 characters is completed. Data transfer and control interface lines are defined below.

D. 3. 1. 2. 4. 1. 1 Display Input Data Signals

Information to be written into memory is presented on six input lines which normally may be at either logic "1" or a logic "0." When the Data Time Line (D. 3. 1. 2. 4. 1. 2) and Write Line (D. 3. 1. 2. 4. 1. 3) are pulsed, the information on these lines will be transferred into memory. Data on these lines must be present and remain unchanged for the entire write time. During data input, these lines are positive logic.

D. 3. 1. 2. 4. 1. 2 Read/Write Data Time

A logic "1" is required on this line to signify that data can be written into memory. Minimum duration of this signal is 300 nanoseconds.

D. 3. 1. 2. 4. 1. 3 Write

A logic "1" is required on this line to permit data entry into memory. This logical "1" pulse must begin with the leading edge of the Read/Write Data Time pulse (D. 3. 1. 2. 4. 1. 2). Data must be present on the input data lines coincident with the Write pulse. The Write pulse shall have a minimum length of 1. 5 microseconds.

D. 3. 1. 2. 4. 1. 4 Clear

A logical "0" signal on this interface causes blank codes to be written into all memory locations thus clearing the panel. Signal pulse width shall be 300 nanoseconds minimum. In addition, no read/write action is to be taken for the duration of clearing memory - 448 microseconds following initiation of a clear pulse.

D. 3. 1. 2. 4. 1. 5 Home

A logical "0" returns cursor to "home" position (row one, column one) without affecting data content. Pulse width shall be 75 nanoseconds minimum.

D. 3. 1. 2. 4. 1. 6 Data Taken/Ready Output

A logical "1" signal from the display to the DIA indicating that the display is ready to accept new data on the input lines. Signal duration is 250 nanoseconds. Timing of these signals is shown in Figure D-4.

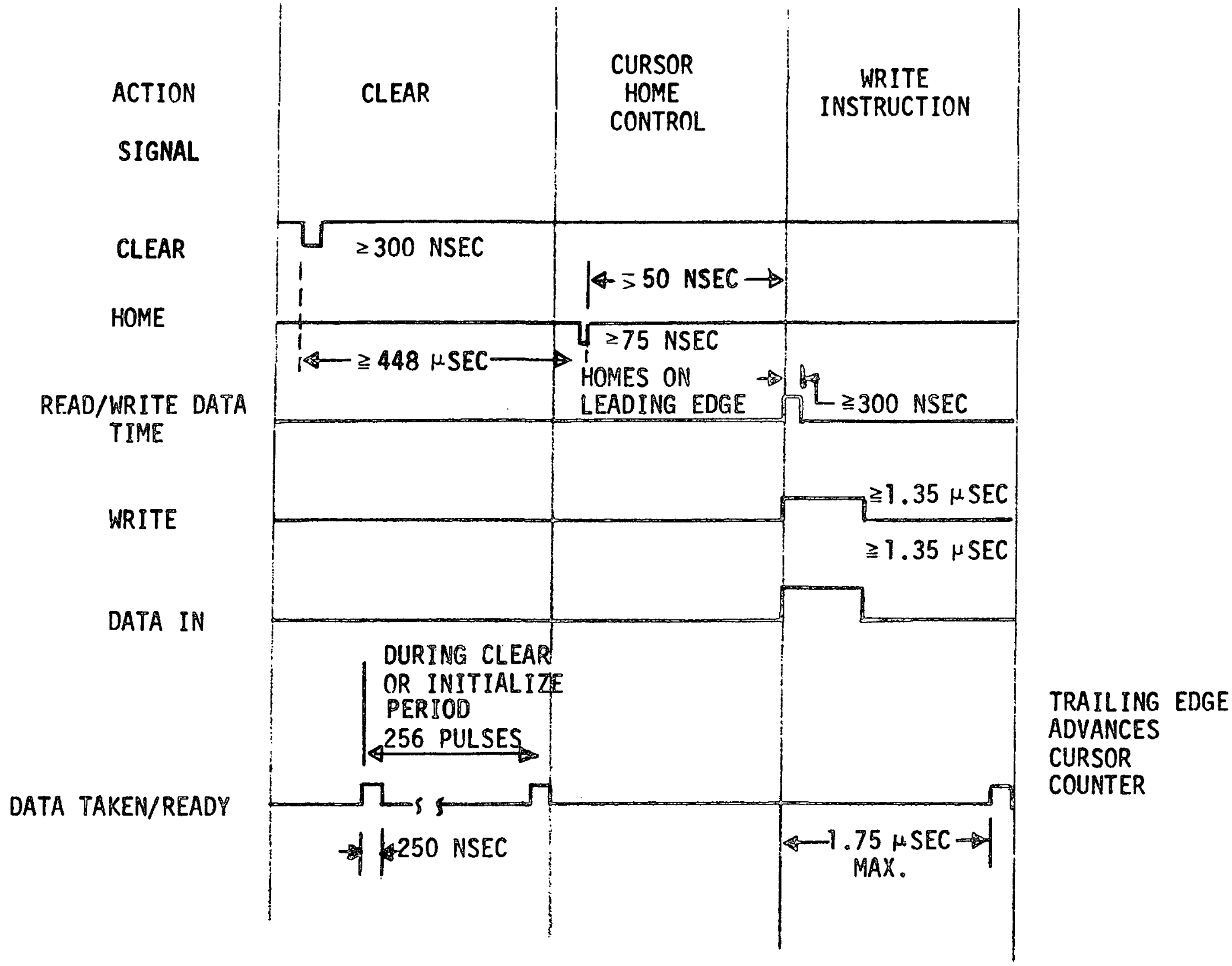


Figure D-4. Programmable Functional Keyboard Display Timing Diagram

In the event that this signal is not received by the DIA within 2 microsecond, the system error bit in the Status Register shall be set.

D. 3. 1. 2. 4. 1. 7 Power Supply Requirements

The following power supply voltages are required for the display unit and shall be provided by MDAC.

+5. 0 vdc ± 5% at 2. 5A	+30. 0 vdc ± 5% at 0. 1A
-12. 0 vdc ± 5% at 0. 5A	-250. 0 vdc ± 5% at 0. 1A

D. 3. 1. 2. 4. 1. 8 Logic Voltage Levels

All logic signals shall be TTL compatible and are defined as follows:

Inputs

Logic "0" = 0. 8V maximum

Logic "1" = 2. 0V minimum

Outputs

Logic "0" = 0. 4V maximum

Logic "1" = 2. 4 V minimum

D. 3. 1. 2. 4. 2 Keyboard Switch Interface Signals

The keyboard switches on the PFK shall permit the operator to generate specific discrete signals for inputting commands to the host computer. These switch input commands in conjunction with the computer and its internal programming allow direct man-machine communication via a selection "menu" display presentation and associated selection keys. There are 8 pushbutton switches associated with the display item selection (variable function) and 10 additional switches associated with specific function selection. Each of these switches also contains integral lights for feedback information. The DIA interface with these pushbutton switches is defined in this section.

D. 3. 1. 2. 4. 2. 1 Switch Contacts

Each of the pushbutton switches will be of the single-pole, single-throw, momentary-contact, pushbutton type. One side of each switch will be connected to a common bus. A power or circuit ground connection shall be provided to this bus by the DIA. The other side of each switch will be connected by individual wires to the DIA. Required voltage and currents shall be supplied by the DIA. The maximum contact resistance measured across the switch contact shall be no greater than 0. 100 ohms when measured at a current of 100 milliamps and 6 VDC. The DIA shall encode and transfer the state of these switches to the DBT upon command and shall be capable of proper operation with contact bounce time during switch activation of up to 10. 0 milliseconds. The DBT logic shall be capable of "remembering" switch contact closures as short as 100 milliseconds. The DIA shall be capable of recognizing switch operations and enabling transfer of switch status information to the DBT within 100 microseconds maximum of initial contact closure.

D. 3. 1. 2. 4. 2. 2 Illuminated Pushbutton

The DIA shall provide decode and current drive capability for integral illumination of all pushbutton switches in response to inputs received via the DBT. Each pushbutton light indicator shall operate at 28 ± 4 VDC and will require a maximum of 40 ± 5 mA at 28 VDC. Power to illuminate the pushbutton indicators shall be provided by the DIA.

D. 3. 1. 2. 4. 2. 3 Connector/Pin Assignments

The interface connector and pin assignments shall be as defined in Table D-7.

D. 3. 1. 2. 5 Event Timer

The Event Timer has the capability of performing count-up or count-down timing operations, using the 1-BPS output from the calendar clock as the count source. Capability to preset the timer for countdown operations and to start, stop, and reset the device remotely via the data bus shall be provided by the DIA. The event timer will contain four digits, each requiring preset via the DIA.

D. 3. 1. 2. 5. 1 Interface Requirements

The timer requires three control inputs identified as Start, Stop, and Reset. These signals shall normally be at logic level "1." Upon receipt of the

Table D-7

PROGRAMMABLE FUNCTION KEYBOARD

J5-Display P/N 450-16-26PN				J6-Keyboard Switches P/N 450-20-41-SN			
Pin	Function	Pin	Function	Pin	Function	Pin	Function
A	Not Used	a	Not Used	A	Not Used	a	Indicator 1
B	Not Used	b	Not Used	B	Switch Com	b	Indicator 2
C	Not Used	c	Not Used	C	Switch 1	c	Indicator 3
D	Not Used			D	Switch 2	d	Indicator 4
E	Not Used			E	Switch 3	e	Indicator 5
F	Not Used			F	Switch 4	f	Indicator 6
G	Sig Grd			G	Switch 5	g	Indicator 7
H	P/S Grd			H	Switch 6	h	Indicator 8
J	Not Used			J	Switch 7	i	Indicator 9
K	-12 VDC			K	Switch 8	j	Indicator 10
L	Not Used			L	Switch 9	k	Indicator 11
M	+5 VDC			M	Switch 10	m	Indicator 12
N	Data Taken/ Ready			N	Switch 11	n	Indicator 13
P	Home			P	Switch 12	p	Indicator 14
R	Clear			R	Switch 13	q	Indicator 15
S	Write			S	Switch 14	r	Indicator 16
T	RnW Data Time			T	Switch 15	s	Indicator 17
U	Data Bit 1			U	Switch 16	t	Indicator 18
V	Data Bit 2				Switch 17		
W	Data Bit 3			W	Switch 18		
X	Data Bit 4			X	Not Used		
Y	Data Bit 5			Y	Not Used		
Z	Data Bit 6			Z	Indicator Common		

appropriate data bus command, the selected control line shall be switched to logic level "0" for a minimum of 10 microseconds. Inputs to the timer shall be standard TTL levels operating into 7400 series logic elements. An additional two inputs for count direction is required input while holding the other input at logic level "1." Circuitry shall be provided to assure non-concidence of count direction signals.

The DIA shall also provide inputs to preset the timer. These shall be in the form of four parallel BCD characters requiring four lines per digit. Inputs are standard TTL levels operating into 7400 series logic elements. Gating of the preset inputs to the timer is accomplished by switching the "Reset" command to logic level "0" for a minimum of 10 microseconds while maintaining the preset lines in the desired state. The DIA shall perform this function automatically upon receipt of the preset command.

Circuit ground for the control and the preset signals shall be referenced to a ground connection on the Event Timer.

D. 3. 1. 2. 5. 2 Connector/Pin Assignment

The Event Timer interface connector on the DIA shall be common with the Calendar Clock Connector (D. 3. 1. 2. 6). The connector type shall be Deutsch Part No. 450-16-26-SN. Pin assignments shall be as specified in Table D-8.

D. 3. 1. 2. 6 Calendar Clock

The DIA shall provide decoding and output of discrete signals to control a Digital Calendar Clock. The Clock has the capability of accumulating and displaying time in seconds, minutes, hours, and days using an internal timing reference. Control signals to start, stop, and reset the Clock are generated by the DIA in response to commands received via the data bus.

D. 3. 1. 2. 6. 1 Interface Requirements

The Calendar Clock requires two control inputs, identified as Run/Hold and Reset. The Run/Hold input requires a continuous TTL logic level signal, logic level "0" for Hold and logic level "1" for Run. The Reset input requires

Table D-8

CLOCK AND TIMER, DEUTSCH 450-16-26SN

Pin	J7	Function
A		Calendar Clock Run/Hold
B		Calendar Clock Reset
C		Calendar Clock Signal Return
D		Count Fwd. Signal
E		Count Reverse Signal
F		Count Direction Common
G		Event Timer Start
H		Event Timer Stop
J		Event Timer - Reset
K		Event Timer Preset 1
L		Event Timer Preset 2
M		Event Timer Preset 3
N		Event Timer Preset 4
P		Event Timer Preset 5
R		Event Timer Preset 6
S		Event Timer Preset 7
T		Event Timer Preset 8
U		Event Timer Preset 9
V		Event Timer Preset 10
W		Event Timer Preset 11
X		Event Timer Preset 12
Y		Event Timer Preset 13
Z		Event Timer Preset 14
a		Event Timer Preset 15
b		Event Timer Preset 16
c		Event Timer Signal Return

a logic level "0" pulse of 10 microseconds minimum duration for reset, and should otherwise be at logic level "1." The loads on both inputs are equivalent to one 7400 series nand gate. All signals shall be referenced to a common signal ground connection on the Calendar Clock.

D. 3. 1. 2. 6. 2 Connector/Pin Assignment

The Calendar Clock interface connector on the DIA shall be common with the Event Timer connector. Pin assignments shall be as specified in Table D-8.

D. 3. 1. 2. 7 Discrete Switches

The DIA shall accept, recognize, and decode discrete command inputs from eight manual switches and transfer the state of these switches to the DBT upon command.

D. 3. 1. 2. 7. 1 Switch Contacts

Each of the eight switches will be a single-pole double-throw toggle type with either momentary or maintained contacts. The wiper of each switch will be connected to a common bus. A power or circuit ground connection shall be provided to this bus by the DIA. The two contacts of each switch will be connected by individual wires to the DIA. The DIA shall be capable of "remembering" switch contact closures on either contact as short as 100 milliseconds and shall provide the capability of indicating to the DBT switch position status at any time through a switch status register.

D. 3. 1. 2. 7. 2 Connector/Pin Assignment

The discrete Switch interface on the DIA shall be common with the Discrete Switch and Analog Meter interfaces. The connector shall be Deutsch Part No. 450-20-41-PN. Pin assignments shall be as defined in Table D-9.

D. 3. 1. 2. 8 Discrete Indicators

The DIA shall provide decode and current drive capability for eight discrete indicator lights in response to inputs received via the DBT.

D. 3. 1. 2. 8. 1 Interface Requirements

Each of the eight indicators will operate at 28 ± 4 VDC, and will require a maximum of 80 ± 12 ma at 28 VDC. Power to illuminate the indicators shall be provided by the DIA.

Table D-9

(J8) DEUTSCH 450-20-41-PN DISCRETE SWITCHES, INDICATORS, AND ANALOG METERS

Pin	Function	Pin	Function
A	Not Used	Y	Indicator 1
B	Not Used	Z	Indicator 2
C	Not Used	a	Indicator 3
D	Not Used	b	Indicator 4
E	Switch 1 N. O.	c	Indicator 5
F	Switch 1 N. C.	d	Indicator 6
G	Switch 2 N. O.	e	Indicator 7
H	Switch 2 N. C.	f	Indicator 8
J	Switch 3 N. O.	g	Indicator common
K	Switch 3 N. C.	h	Lamp Test
L	Switch 4 N. O.	i	Lamp Test common
M	Switch 4 N. C.	j	Not Used
N	Switch 5 N. O.	k	Meter 1 positive
P	Switch 5 N. C.	m	Meter 1 negative
R	Switch 6 N. O.	n	Meter 2 positive
S	Switch 6 N. C.	p	Meter 2 negative
T	Switch 7 N. O.	q	Meter 3 positive
U	Switch 7 N. C.	r	Meter 3 negative
V	Switch 8 N. O.	s	Meter 4 positive
W	Switch 8 N. C.	t	Meter 4 negative
X	Switch common		

D. 3. 1. 2. 8. 2 Connector/Pin Assignment

The Discrete Indicator interface connector of the DIA shall be common to the Discrete Switch interface described in D. 2. 1. 2. 7. Pin assignments shall be as defined in Table D-9.

D. 3. 1. 2. 9 Analog Meters

The DIA shall interface with four discrete meters with expansion to eight meters easily accomplished. Meter commands will be input to the DIA via the DBT in the form of 8-bit (or more) level codes, accompanied by a digitally coded address to select the appropriate meter. The DIA shall decode the address, convert the 8-bit level code to the appropriate DC voltage, and provide the drive signal to the meter movement. Capability shall be provided to drive all eight meters simultaneously and continuously.

D. 3. 1. 2. 9. 1 Interface Requirements

Each of the eight meters will have a 0 to 5 VDC movement requiring 1 ma maximum for full-scale deflection. Conversion accuracy from the digital level code to the analog output shall be ±1 percent or better.

D. 3. 1. 2. 9. 2 Connector/Pin Assignment

The Analog Meter interface connector on the DIA shall be common with the Discrete Switch connector (D. 3. 1. 2. 7). Pin assignments shall be as specified in Table D-9.

D. 3. 1. 2. 10 Status

Upon receipt of the Status Register address, the DIA shall transfer the contents of the status register to the DBT. Status bits which represent past events, such as parity error, shall then be reset.

D. 3. 1. 2. 11 Power Supplies

Power supplies required for operation of the DIA shall be provided as part of the DIA. In addition, power supplies for operation of the following display equipment shall be provided:

A. Programmable functional keyboard display, pushbutton switches, and indicator lights (D. 3. 1. 2. 4. 2. 1 and D. 3. 1. 2. 4. 2. 2).
   The other voltages are to be supplied by external equipment.
B. Discrete switches (D. 3. 1. 2. 7. 1).
C. Discrete indicators (D. 3. 1. 2. 8. 1).
D. Analog meters (D. 3. 1. 2. 9. 1).

The DIA shall operate from standard single-phase power, 115 VAC (RMS), ±10 volts, 60 Hz, ±1.5 Hz. Input power shall not exceed 175 watts. Power input shall be through connector J11 and shall be a Deutsch Part No. 450-14-4P with the following pin assignment:

A - 117 vac	C - equipment ground
B - neutral	D - not used

D. 3. 1. 2. 12 Isolation and Grounding

The DBT shall accept signal ground connections from interfacing display devices and provide a single-point ground. The DIA signal ground shall also be connected to the single-point ground. Provisions for attaching this single-point ground to the frame shall be provided. When the DIA signal ground is disconnected, isolation between the DIA chassis and signal ground shall be 2 megohms at 25 VDC. All signal grounds shall also be mutually isolated from power ground by 2 megohms at 25 VDC.

D. 3. 1. 2. 13 Future Growth Provisions

The VTE shall provide a spare (growth) serial output port which will output the data received from the DBT upon proper address decoding. The data rate for this output shall be at the same rate as that received at the DBT input. Outputs shall be standard TTL logic level signals operating into 7400 series logic elements. Capability to easily add duplex operation (two-way data transfer) to this growth channel shall be provided. No DC isolation is required. The connector shall be Deutsch Part No. 450-14-12PN. P/N assignments shall be as defined in Table D-10. In addition, the DIA shall have adequate unused volume and power supply capability to permit future expansion. As a minimum, expansion capability for allowing two additional circuit cards and 20-percent power supply availability shall be provided.

D. 3. 1. 2. 14 Self-Test Provisions

The DIA shall include self test and fault isolation capability as defined in the following sections.

Table D-10

DEUTSCH PART NUMBER 450-14-12PN PIN ASSIGNMENTS

J10 Pin	Growth Function
A	Data
B	Gated Clcok
C	Signal Return
D	Not Used
E	Not Used
F	Not Used
G	Not Used
H	Not Used
J	Not Used
K	Not Used
L	Not Used
M	Not Used

D. 3. 1. 2. 14. 1 Test Clock

Provision shall be made for accepting a test clock signal from an external source such as a laboratory-type pulse generator. This clock may be at any rate from a single pulse up to a maximum of 1 MBPS. The test clock input shall bypass the bilevel NRZ and invalid clock detection circuitry and shall be at standard TTL levels. The input load shall be equivalent to one 7400 series logic gate.

D. 3. 1. 2. 14. 2 Test Data

Provisions shall be made for accepting a test data input from an external source. This data input may be at any rate from 0 up to 1 MBPS. The data input shall bypass the bilevel NRZ detection circuitry and shall be at standard TTL levels. The input load shall be equivalent to one 7400 series logic gate.

D. 3. 1. 2. 14. 3 PDS-1 Data

The DIA shall be capable of taking data in the form of 16-bit parallel words from the PDS-1 output and placing them in the DIA receiving register. From that point, the words will be decoded and treated as if they had come from the Data Bus Terminal. This will permit addressing of other display devices from the PDS-1 and thereby performing a self test of the console. Self-test data will be differentiated from normal data by a unique device selection code I0A7 and I0B7 from the PDS-1. When in the self-test mode, normal data inputs to the PDS-1 shall be disabled. The clock source while in this mode may be either the normal clock from the data bus terminal or the Test Clock defined in D. 3. 1. 2. 14. 1.

D. 3. 1. 2. 14. 4 Lamp Test

The PFK pushbutton switch indicators and the discrete event light circuits shall be designed to permit lamp testing when a remote switch is activated. This will require activation of the lamp driver circuits via the panel-mounted switch.

D. 3. 2 Operating Equipment

The DIA shall be designed to operate in a laboratory environment under the following conditions:

A. Ambient Temperature — +10° to +30° C
B. Barometric Pressure — Sea level to 5, 000 feet
C. Relative Humidity — 10 to 80 percent

D. 3. 3 Packaging

The DIA shall be packaged in a modular fashion to permit maintenance/repair as well as provide for ease of growth. The equipment shall be designed to mount within a MIL-STD-189, 19-inch equipment rack with equipment slide capability. All logic cards and modules shall be of a plug-in nature to facilitate fast replacement or addition. Maximum chassis depth shall not exceed 20 inches (excluding rear-mounted connector) or 3.5 inches in height. The equipment slides shall be provided. Weight shall be less than 30 pounds. Connectors shall be accessible from the rear. No special cooling shall be required.

D.4 QUALITY AND RELIABILITY

The construction of the DIA will reflect good standard practices. Commercially available parts such as plastic encapsulated semiconductors are acceptable; however, the use of parts that have the best chance of being available in high-reliability equivalents is recommended.

D.5 DOCUMENTATION

Documentation on the design, operation, and fault isolation is required. As a minimum, the following are required:

A. Functional Description
B. Operating Instructions
C. Electrical Schematics
D. Fault Isolation Description
E. Parts Lists
F. Programming Guide